

# MPS5172

## General Purpose Transistor NPN Silicon

### Features

- Pb-Free Packages are Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	25	Vdc
Collector-Base Voltage	$V_{CBO}$	25	Vdc
Emitter-Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current - Continuous	$I_C$	100	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	625 5.0	mW mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 60^\circ\text{C}$	$P_D$	450	mW
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 12	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	200	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	83.3	$^\circ\text{C}/\text{W}$

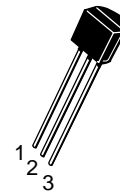
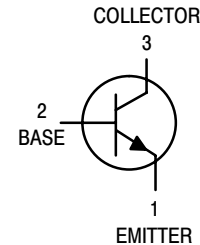
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



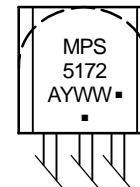
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TO-92 (TO-226)  
CASE 29  
STYLE 1

### MARKING DIAGRAM



MPS5172 = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping
MPS5172	TO-92	5000 / Bulk
MPS5172G	TO-92 (Pb-Free)	5000 / Bulk
MPS5172RLRM	TO-92	2000/Ammo Pack
MPS5172RLRMG	TO-92 (Pb-Free)	2000/Ammo Pack

# MPS5172

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Breakdown Voltage (Note 1) ( $I_C = 10\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	25	–	Vdc
Collector Cutoff Current ( $V_{CE} = 25\text{ V}$ , $I_B = 0$ )	$I_{CES}$	–	100	nAdc
Collector Cutoff Current ( $V_{CB} = 25\text{ V}$ , $I_E = 0$ ) ( $V_{CB} = 25\text{ V}$ , $I_E = 0$ , $T_A = 100^\circ\text{C}$ )	$I_{CBO}$	– –	100 10	nAdc $\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	–	100	nAdc
<b>ON CHARACTERISTICS (Note 1)</b>				
DC Current Gain ( $V_{CE} = 10\text{ V}$ , $I_C = 10\text{ mA}$ )	$h_{FE}$	100	500	–
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mAdc}$ , $I_B = 1.0\text{ mAdc}$ )	$V_{CE(sat)}$	–	0.25	Vdc
Base–Emitter On Voltage ( $I_C = 10\text{ mAdc}$ , $V_{CE} = 10\text{ V}$ )	$V_{BE(on)}$	0.5	1.25	Vdc
<b>SMALL–SIGNAL CHARACTERISTICS</b>				
Collector–Base Capacitance ( $V_{CB} = 10\text{ V}$ , $f = 1.0\text{ MHz}$ )	$C_{cb}$	1.6	10	pF
Small–Signal Current Gain ( $I_C = 10\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	100	750	–

1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

TYPICAL STATIC CHARACTERISTICS

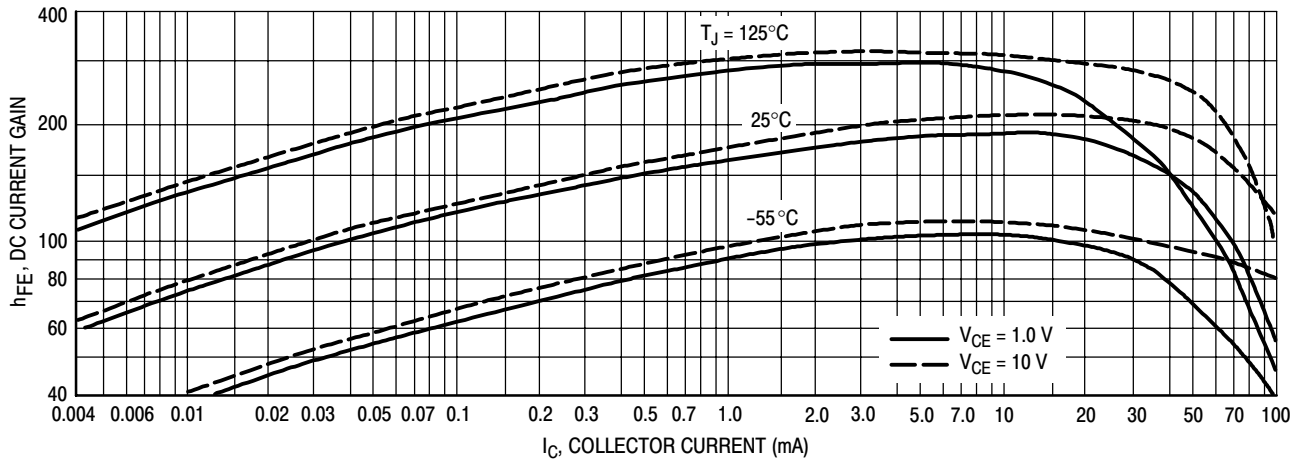


Figure 1. DC Current Gain

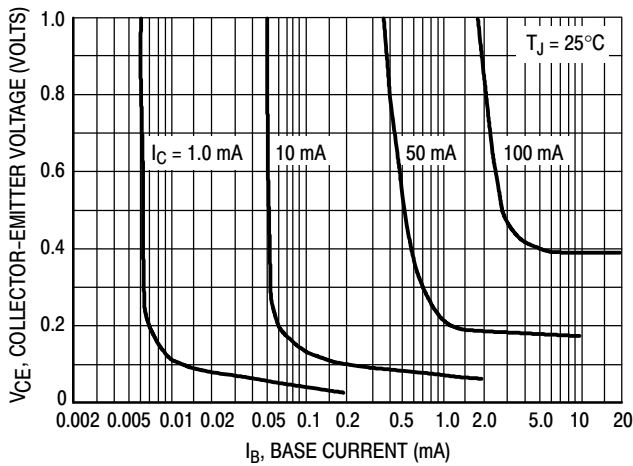


Figure 2. Collector Saturation Region

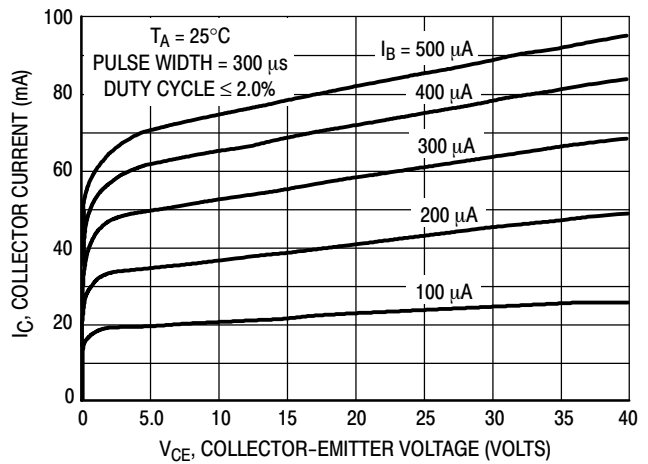


Figure 3. Collector Characteristics

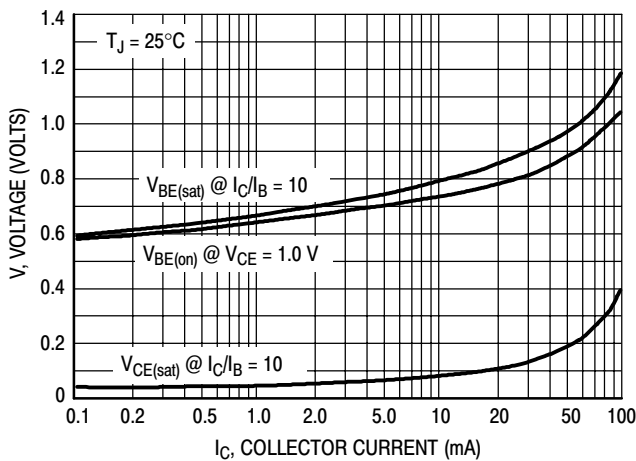


Figure 4. "On" Voltages

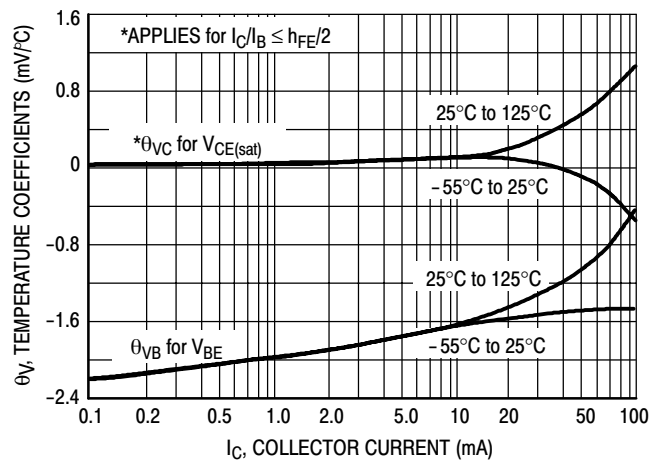


Figure 5. Temperature Coefficients

TYPICAL DYNAMIC CHARACTERISTICS

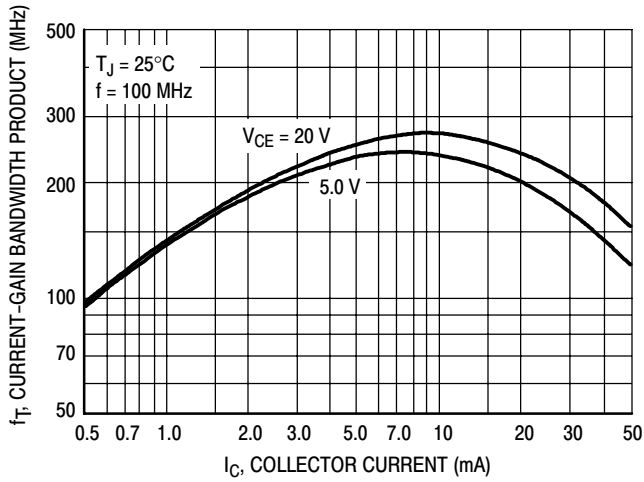


Figure 6. Current-Gain - Bandwidth Product

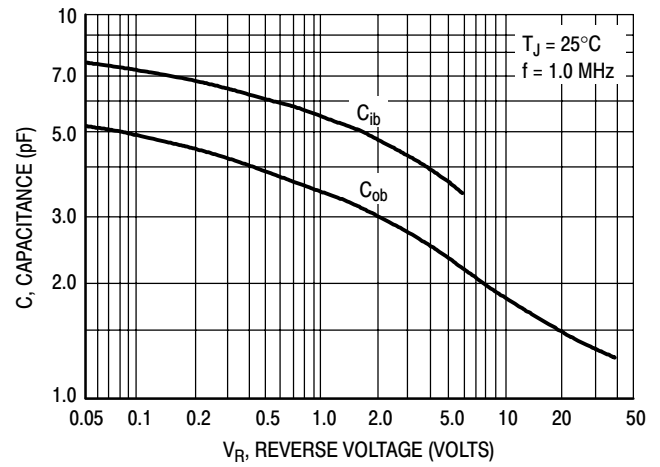


Figure 7. Capacitance

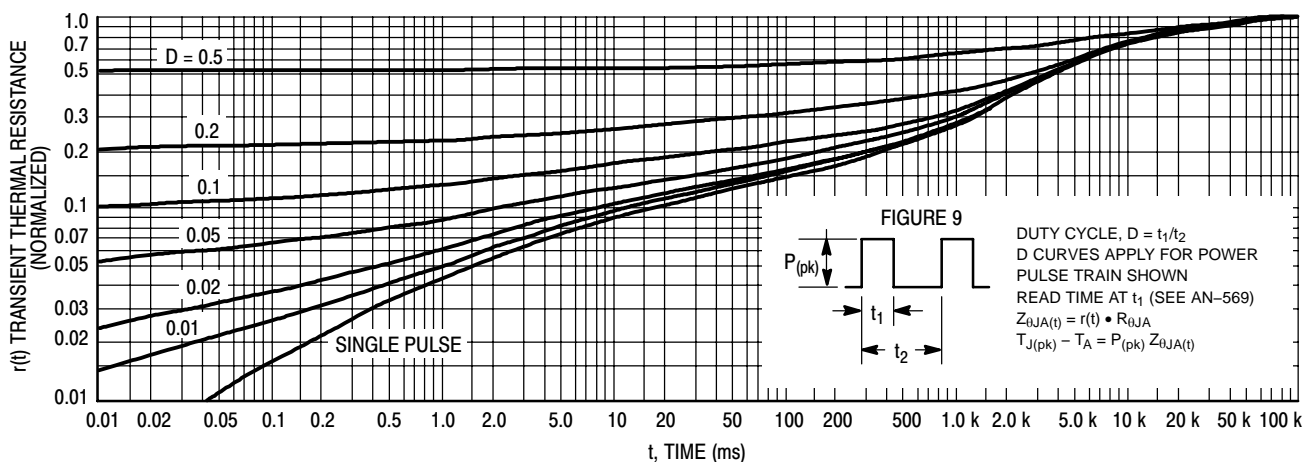


Figure 8. Thermal Response

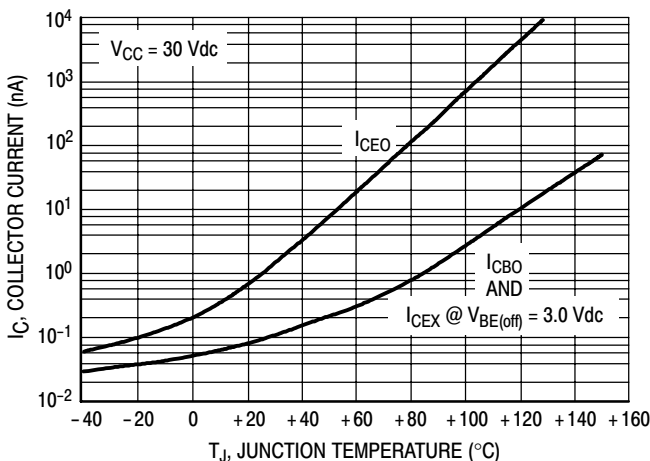


Figure 10.

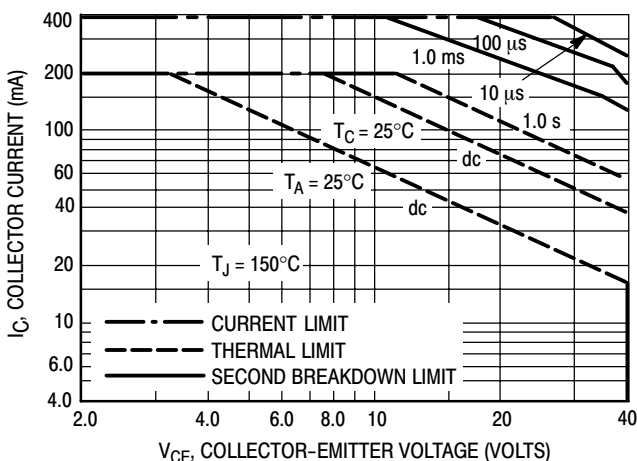


Figure 11.

**DESIGN NOTE: USE OF THERMAL RESPONSE DATA**

A train of periodical power pulses can be represented by the model as shown in Figure 9. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 8 was calculated for various duty cycles.

To find  $Z_{\theta JA(t)}$ , multiply the value obtained from Figure 8 by the steady state value  $R_{\theta JA}$ .

Example:

The MPS3904 is dissipating 2.0 watts peak under the following conditions:

$$t_1 = 1.0 \text{ ms}, t_2 = 5.0 \text{ ms. (D = 0.2)}$$

Using Figure 8 at a pulse width of 1.0 ms and  $D = 0.2$ , the reading of  $r(t)$  is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^\circ\text{C}.$$

For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at [www.onsemi.com](http://www.onsemi.com).

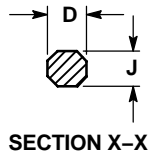
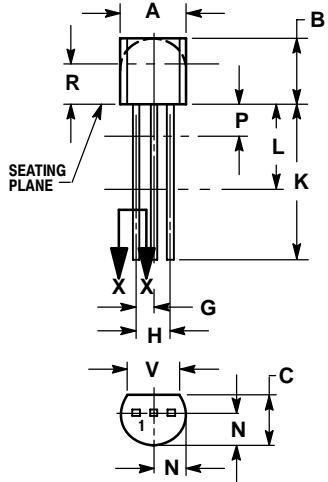
The safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 11 is based upon  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  or  $T_A$  is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 8. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MPS5172

## PACKAGE DIMENSIONS

TO-92 (TO-226)  
CASE 29-11  
ISSUE AL



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 1:

1. EMITTER
2. BASE
3. COLLECTOR
3. SOURCE

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