MITEL Technical Data

MD4311B/4511B

CMOS/MSI 7-SEGMENT DECODER/DRIVER/LATCH

FEB. 79

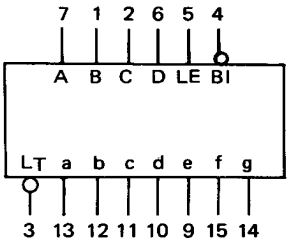
DESCRIPTION

The 4311B/4511B are CMOS/MSI 7-Segment Decoder Driver incorporating input latches and bipolar NPN output circuits, where each segment is capable of sourcing over 25 mAdc of current to drive LED, incadescent, fluorescent, gas discharge or LCD displays. See back page for part numbers.

CMOS POWER CONSUMPTION (25 nW typ.)
EITHER BCD OR HEXADECIMAL CODES
HIGH SPEED INPUT LATCHES FOR DATA STORAGE JEDEC-B SPEC. 3 VOLT TO 18 VOLT CMOS OPERATION TIME SHARE CAPABILITY.

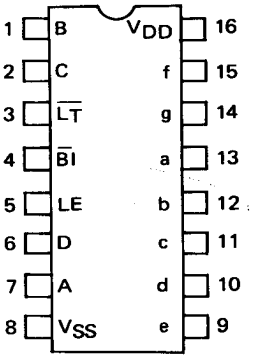
4511B SAME AS 14511 OR 4511 TYPES.

LOGIC SYMBOL



V_{DD} = PIN 16
V_{SS} = Pin 8

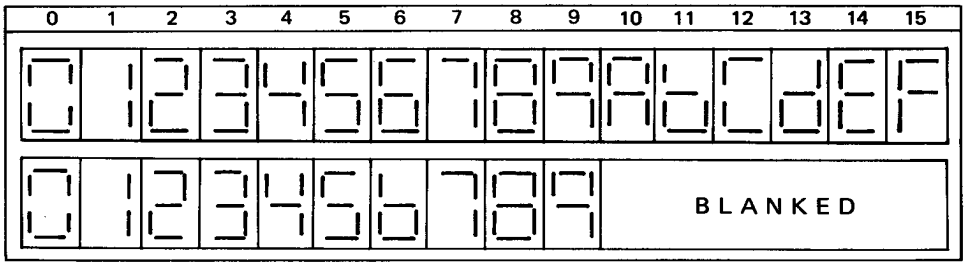
CONNECTION DIAGRAM
DIP (TOP VIEW)



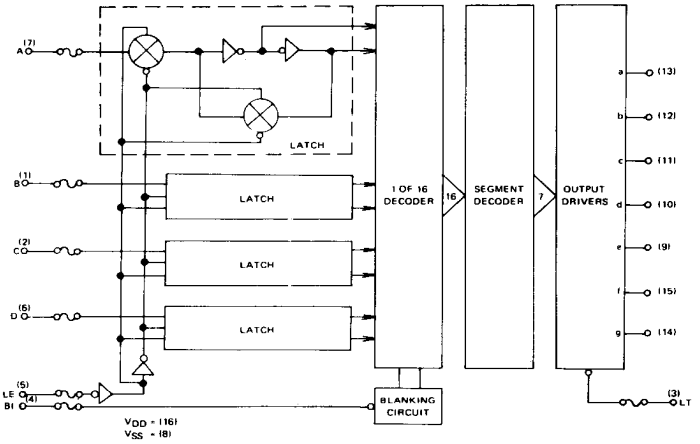
PIN NAMES

A_1, B_1, C_1, D	Address (Data) Inputs
LE	Latch Enable (Active HIGH) Input
$\overline{BI}$	Blanking (Active LOW) Input
$\overline{LT}$	Lamp Test (Active LOW) Input
a, b, c, d, e, f, g	(Active HIGH) Outputs

NUMERICAL DESIGNATIONS



BLOCK DIAGRAM
4311B/4511B



ORIG MIT
002980
53 2980

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FUNCTIONAL DESCRIPTION

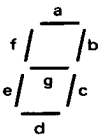
The 4311B and 4511B are CMOS/MSI 7-Segment Decoder Drivers which provide the function of a 4-bit storage latch with either an 8421 BCD-to-seven segment decoder (4511B) or an 8421 Hexadecimal-to-seven segment decoder (4311B), and an output source current capability of greater than 50mA in pulsed mode.

Lamp test ($\overline{LT}$), blanking ($\overline{BI}$) and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a 8421 code, respectively.

The latches on the four data inputs (A, B, C, D) are controlled by an active HIGH latch enable LE. When LE is LOW, the state of the outputs is determined by the input data. When LE goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. (Latch enabled).

TRUTH TABLE

DISPLAY	INPUTS							OUTPUTS														
								4311B							4511B							
	LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	a	b	c	d	e	f	g
–	H	H	H	X	X	X	X	STABLE							STABLE							
BLANK	X	L	H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
8	X	X	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	L	H	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
1	L	H	H	L	L	L	H	L	H	H	L	L	L	L	L	H	H	L	L	L	L	L
2	L	H	H	L	L	H	L	H	H	L	H	H	L	H	H	H	L	H	H	L	H	H
3	L	H	H	L	L	H	H	H	H	H	H	L	L	H	H	H	H	H	L	L	H	H
4	L	H	H	L	H	L	L	L	H	H	L	L	H	H	L	H	H	L	L	H	H	H
5	L	H	H	L	H	L	H	H	L	H	H	L	H	H	H	L	H	H	L	H	H	H
6	L	H	H	L	H	H	L	H	L	H	H	H	H	H	L	L	H	H	H	H	H	H
7	L	H	H	L	H	H	H	H	H	H	L	L	L	L	H	H	H	L	L	L	L	L
8	L	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
9	L	H	H	H	L	L	H	H	H	H	H	L	H	H	H	H	H	L	L	H	H	H
A*	L	H	H	H	L	H	L	H	H	H	L	H	H	H	L	L	L	L	L	L	L	L
B*	L	H	H	H	L	H	H	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L
C*	L	H	H	H	H	L	L	H	L	L	H	H	H	L	L	L	L	L	L	L	L	L
D*	L	H	H	H	H	L	H	L	H	H	H	H	L	H	L	L	L	L	L	L	L	L
E*	L	H	H	H	H	H	L	H	L	L	H	H	H	H	L	L	L	L	L	L	L	L
F*	L	H	H	H	H	H	H	H	L	L	L	H	H	H	L	L	L	L	L	L	L	L



* Blanked for 4511B
** Don't care For 4511B

DEFINITION	INPUTS	OUTPUTS
H	HIGH Voltage Level	Sourcing Current
L	LOW Voltage Level	Output is "off"
X	Don't Care	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V dc. Storage Temperature -65°C. to 150°C. Operation temperature -40°C. to 85°C. or -55°C. to 125°C.

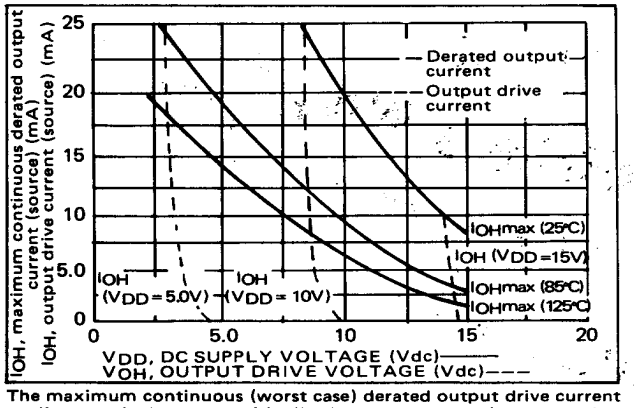
Characteristic	Symbol	VDD Vdc	MILITARY -55°C Min.	MILITARY -55°C Max.	MILITARY +25°C Min.	MILITARY +25°C Typ.	MILITARY +25°C Max.	MILITARY +125°C Min.	MILITARY +125°C Max.	COMMERCIAL -40°C Min.	COMMERCIAL -40°C Max.	COMMERCIAL +25°C Min.	COMMERCIAL +25°C Typ.	COMMERCIAL +25°C Max.	COMMERCIAL -85°C Min.	COMMERCIAL -85°C Max.	Unit
Output Voltage "O" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
		15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level		5.0	4.1	–	4.1	4.57	–	4.1	–	4.1	–	4.1	4.57	–	4.1	–	
		10	9.1	–	9.1	9.58	–	9.1	–	9.1	–	9.1	9.58	–	9.1	–	
		15	–	–	–	14.59	–	–	–	–	–	–	14.59	–	–	–	
Noise Immunity* ($V_{out} \geq$ 3.5Vdc) ($V_{out} \geq$ 7.0Vdc) ($V_{out} \geq$ 10.5Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
		10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq$ 1.5Vdc) ($V_{out} \leq$ 3.0Vdc) ($V_{out} \leq$ 4.5Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
		10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Voltage																	
(I_{OH} = 0 mAdc Source	V_{OH}	5.0	–	–	4.10	4.57	–	–	–	–	–	4.10	4.57	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			–	–	3.90	4.12	–	–	–	–	–	3.60	4.12	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			–	–	3.40	3.75	–	–	–	–	–	2.80	3.75	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	–	–	9.10	9.58	–	–	–	–	–	9.10	9.58	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			–	–	9.0	9.17	–	–	–	–	–	8.75	9.17	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			–	–	8.60	8.90	–	–	–	–	–	8.10	8.90	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	–	–	–	14.59	–	–	–	–	–	–	14.59	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			–	–	–	14.18	–	–	–	–	–	–	14.18	–	–	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			–	–	–	13.95	–	–	–	–	–	–	13.95	–	–	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	–	–	–	13.80	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.5	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_D	5.0	–	25	–	0.025	25	–	1500	–	250	–	0.025	250	–	3500	uW
		10	–	100	–	0.1	100	–	6000	–	1000	–	0.1	1000	–	14000	
		15	–	–	–	0.23	–	–	–	–	–	–	0.23	–	–	–	
Output Rise Time (C_L = 50pF)	t_r	5.0	–	–	–	40	200	–	–	–	–	–	40	250	–	–	ns
		10	–	–	–	30	100	–	–	–	–	–	30	160	–	–	
		15	–	–	–	18	–	–	–	–	–	–	18	–	–	–	
Output Fall Time (C_L = 50pF)	t_f	5.0	–	–	–	200	–	–	–	–	–	–	200	–	–	–	ns
		10	–	–	–	160	–	–	–	–	–	–	160	–	–	–	
		15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	
Propagation Delay Time (Data) (C_L = 50pF)	t_{PLH}	5.0	–	–	–	660	1500	–	–	–	–	–	640	2250	–	–	ns
		10	–	–	–	260	600	–	–	–	–	–	250	900	–	–	
		15	–	–	–	190	–	–	–	–	–	–	175	–	–	–	
	t_{PHL}	5.0	–	–	–	720	1500	–	–	–	–	–	720	2250	–	–	ns
		10	–	–	–	290	600	–	–	–	–	–	290	900	–	–	
		15	–	–	–	195	–	–	–	–	–	–	195	–	–	–	
Propagation Delay Time (Blank (C_L = 50pF)	t_{PLH}	5.0	–	–	–	340	1000	–	–	–	–	–	320	1500	–	–	ns
		10	–	–	–	145	400	–	–	–	–	–	130	600	–	–	
		15	–	–	–	115	–	–	–	–	–	–	100	–	–	–	
	t_{PHL}	5.0	–	–	–	485	1000	–	–	–	–	–	485	1500	–	–	ns
		10	–	–	–	200	400	–	–	–	–	–	200	600	–	–	
		15	–	–	–	160	–	–	–	–	–	–	160	–	–	–	
Propagation Delay Time (Lamp Test) (C_L = 50pF)	t_{PLH}	5.0	–	–	–	290	625	–	–	–	–	–	290	940	–	–	ns
		10	–	–	–	125	250	–	–	–	–	–	125	375	–	–	
		15	–	–	–	85	–	–	–	–	–	–	85	–	–	–	
	t_{PHL}	5.0	–	–	–	290	625	–	–	–	–	–	290	940	–	–	ns
		10	–	–	–	120	250	–	–	–	–	–	120	375	–	–	
		15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Set-Up Time	t_{setup}	5.0	–	–	180	90	–	–	–	–	–	270	90	–	–	–	ns
		10	–	–	76	38	–	–	–	–	–	114	38	–	–	–	
		15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Hold Time	t_{hold}	5.0	–	–	0	-90	–	–	–	–	–	0	-90	–	–	–	ns
		10	–	–	0	-38	–	–	–	–	–	0	-38	–	–	–	
		15	–	–	–	-20	–	–	–	–	–	–	-20	–	–	–	
Minimum Latch Enable Pulse Width	PW_{LE}	5.0	–	–	520	260	–	–	–	–	–	780	260	–	–	–	ns
		10	–	–	220	110	–	–	–	–	–	330	110	–	–	–	
		15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	

*DC Noise Margin (V_{NH} - V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

GUARANTEED OPERATING RANGES

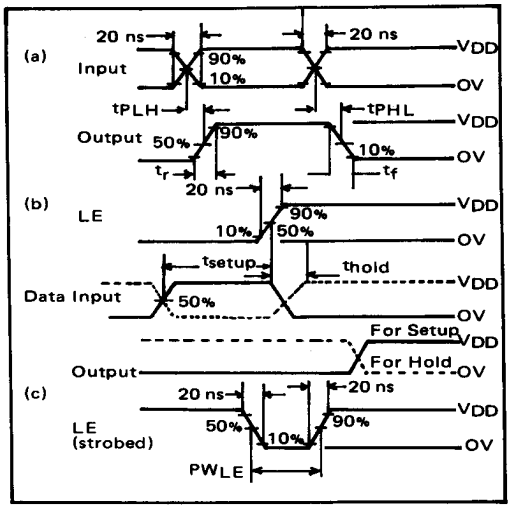
PART NUMBER	VDD			TEMPERATURE	PACKAGE
	MIN.	TYP.	MAX.		
MD4311BE	3V	5V	18V	–40°C to 85°C	Expoxy Dual-in-Line
SIL4511BE	3V	5V	18V	–40°C to 85°C	Expoxy Dual-in-Line
MD4311BC	3V	5V	18V	–40°C to 85°C	Ceramic Dual-in-Line
SIL4511BC	3V	5V	18V	–40°C to 85°C	Ceramic Dual-in-Line
MD4311BF	3V	5V	18V	–55°C to 125°C	Ceramic Dual-in-Line
SIL4511BF	3V	5V	18V	–55°C to 125°C	Ceramic Dual-in-Line
MD4311BI	3V	5V	18V	–55°C to 125°C	Tested Chips-883, 2010B
SIL4511BI	3V	5V	18V	–55°C to 125°C	Tested Chips-883, 2010B
MD4311BH	3V	5V	18V	–40°C to 85°C	Tested Chips-883, 2010B
SIL4511BH	3V	5V	18V	–40°C to 85°C	Tested Chips-883, 2010B

FIGURE 1 – DERATING AND OUTPUT DRIVE CURVES PER OUTPUT

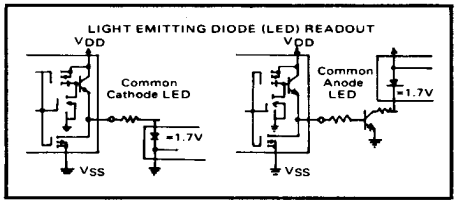


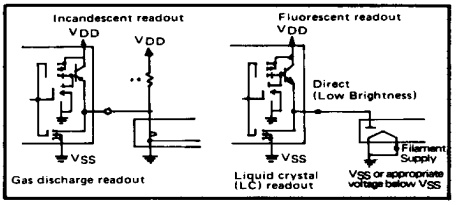
The maximum continuous (worst case) derated output drive current applies to a single output with all other outputs sourcing an equal amount of current. Operation above the derating curve at a given temperature is not recommended.
The output drive curves are typical values.

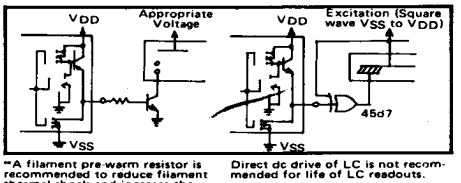
FIGURE 2 DYNAMIC SIGNAL WAVEFORMS



CONNECTIONS TO VARIOUS DISPLAY READOUTS







~A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LC is not recommended for life of LC readouts.

For more information write or phone the leaders in CMOS technology, MITEL Semiconductor:

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