M5M51008BP,FP,VP,RV,KV,KR -55L,-70L,-10L, -55LL,-70LL,-10LL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008BP,FP,VP,RV,KV,KR are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51008BVP,RV,KV,KR are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD).Two types of devices are available. VP,KV(normal lead bend type package),RV,KR(reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

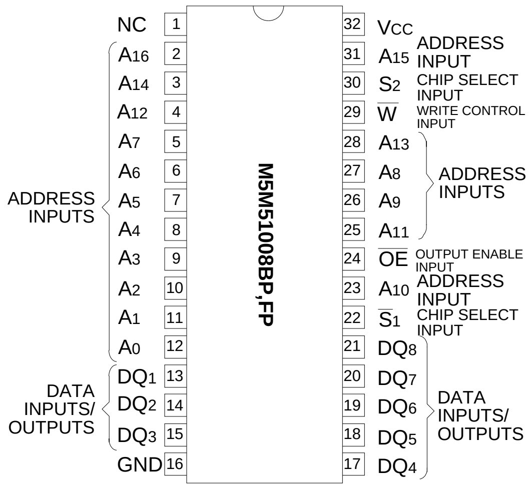
Type name	Access time (max)	Power supply current Active (1MHz) (max)	Power supply current stand-by (max)
M5M51008BP,FP,VP,RV,KV,KR-55L	55ns	15mA	100µA (Vcc=5.5V)
M5M51008BP,FP,VP,RV,KV,KR-70L	70ns		
M5M51008BP,FP,VP,RV,KV,KR-10L	100ns		
M5M51008BP,FP,VP,RV,KV,KR-55LL	55ns	15mA	20µA (Vcc=5.5V) 0.3µA (Vcc=3.0V,typ)
M5M51008BP,FP,VP,RV,KV,KR-70LL	70ns		
M5M51008BP,FP,VP,RV,KV,KR-10LL	100ns		

- Single +5V power supply
- Low stand-by current 0.3µA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S_1}$,S_2
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  - M5M51008BP ············32pin 600mil DIP
  - M5M51008BFP ············32pin 525mil SOP
  - M5M51008BVP,RV ············32pin 8 X 20 mm^2 TSOP
  - M5M51008BKV,KR ············32pin 8 X 13.4 mm^2 TSOP

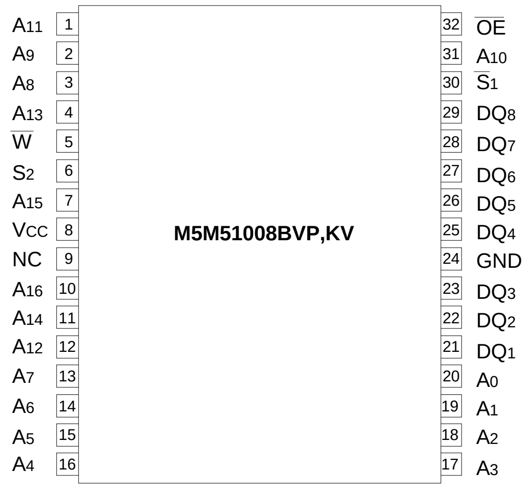
APPLICATION

Small capacity memory units

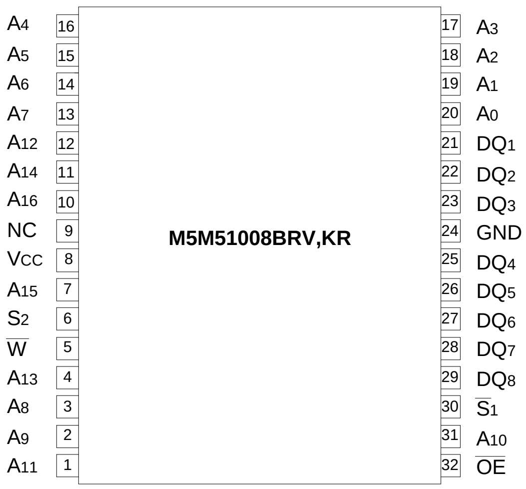
PIN CONFIGURATION (TOP VIEW)



Outline 32P4(P), 32P2M-A(FP)



Outline 32P3H-E(VP), 32P3K-B(KV)



Outline 32P3H-F(RV), 32P3K-C(KR)

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51008B series are determined by a combination of the device control inputs $\overline{S}_1$,S_2,$\overline{W}$ and $\overline{OE}$.

Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$,$\overline{S}_1$ or S_2,whichever occurs first,requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

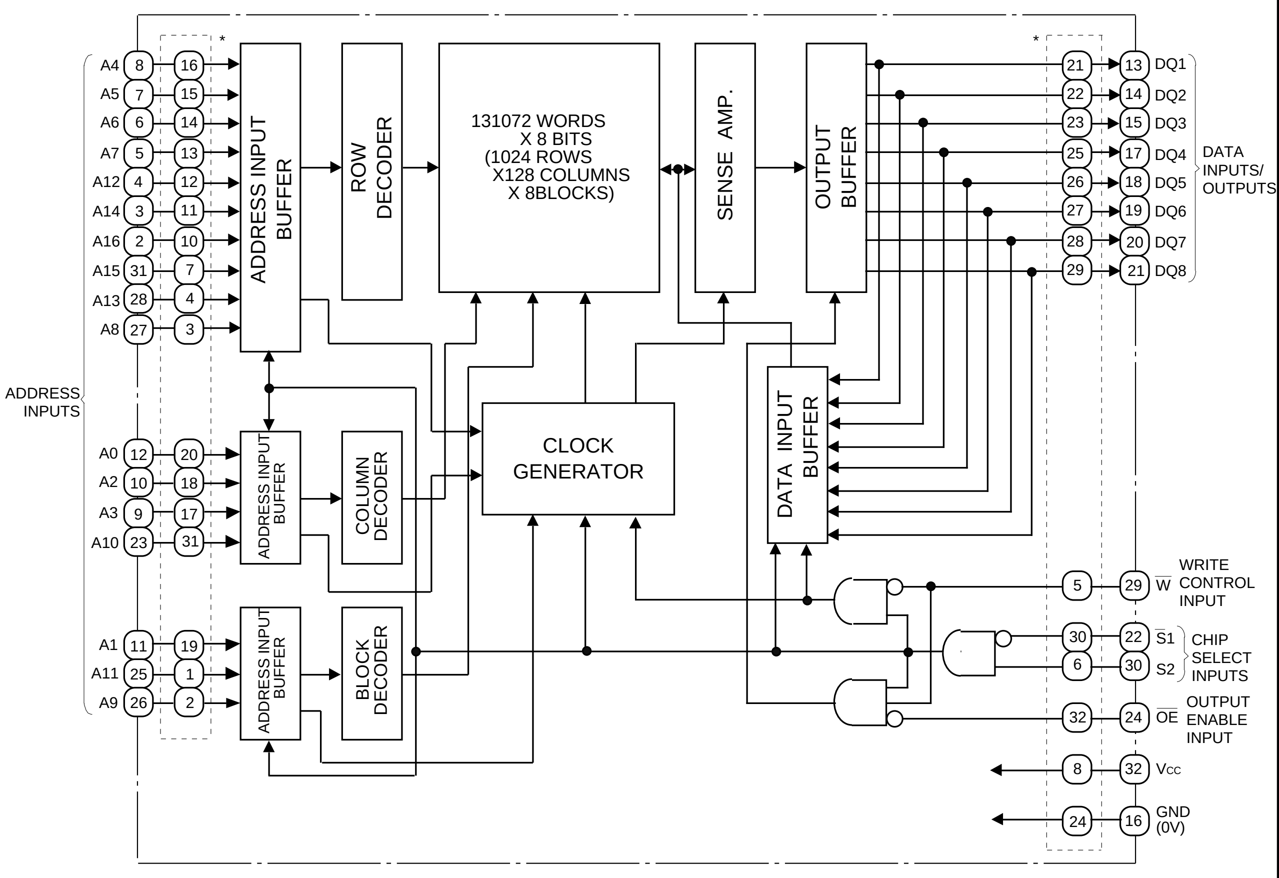
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state($\overline{S}_1$=L,S_2=H).

When setting $\overline{S}_1$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high- impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}_1$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	– 0.3*~7	V
V_I	Input voltage		– 0.3*~Vcc + 0.3	V
V_O	Output voltage		0~Vcc	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		– 65~150	°C

* –3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc +0.3V	V
V_{IL}	Low-level input voltage			–0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH}= –0.5mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}= –0.05mA		Vcc -0.5V			V
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	V
I_I	Input current	V_I=0~Vcc				±1	µA
I_O	Output current in off-state	$\overline{S}_1=V_{IH}$ or $S_2=V_{IL}$ or $OE=V_{IH}$ $V_{I/O}$=0~V_{CC}				±1	µA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}_1$≤0.2V,S_2≥Vcc–0.2V, other inputs≤0.2V or ≥Vcc–0.2V Output-open(duty 100%)	Min cycle		35 (40)**	70 (80)**	mA
			1MHz		4	15	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}_1=V_{IL}$,$S_2=V_{IH}$, other inputs=V_{IH} or V_{IL} Output-open(duty 100%)	Min cycle		38 (43)**	70 (85)**	mA
			1MHz		5	15	
I_{CC3}	Stand-by current	1) S_2 ≤ 0.2V 2) $\overline{S}_1$ ≥ V_{CC}–0.2V, S_2 ≥ V_{CC}–0.2V other inputs=0~V_{CC}	-L			100	µA
			-LL			20	
I_{CC4}	Stand-by current	$\overline{S}_1=V_{IH}$ or $S_2=V_{IL}$, other inputs=0~V_{CC}				3	mA

* –3.0V in case of AC (Pulse width ≤ 30ns)
** inside ( ) is a value of -55L,-55LL

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc = 5V, Ta = 25°C

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ·············· V_{IH}=2.4V,V_{IL}=0.6V (-70L,-10L,-70LL,-10LL)
V_{IH}=3.0V,V_{IL}=0.0V (-55L,-55LL)
Input rise and fall time ····· 5ns
Reference level ················ V_{OH}=V_{OL}=1.5V
Output loads ····················· Fig.1, C_L=100pF (-10L,-10LL,)
C_L=30pF (-55L,-70L,-55LL,-70LL)
C_L=5pF (for t_{en},t_{dis})
Transition is measured ± 500mV from steady state voltage. (for t_{en},t_{dis})

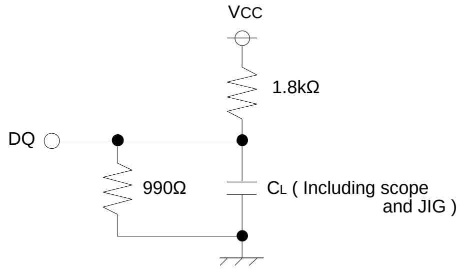


Fig.1 Output load

(2) READ CYCLE

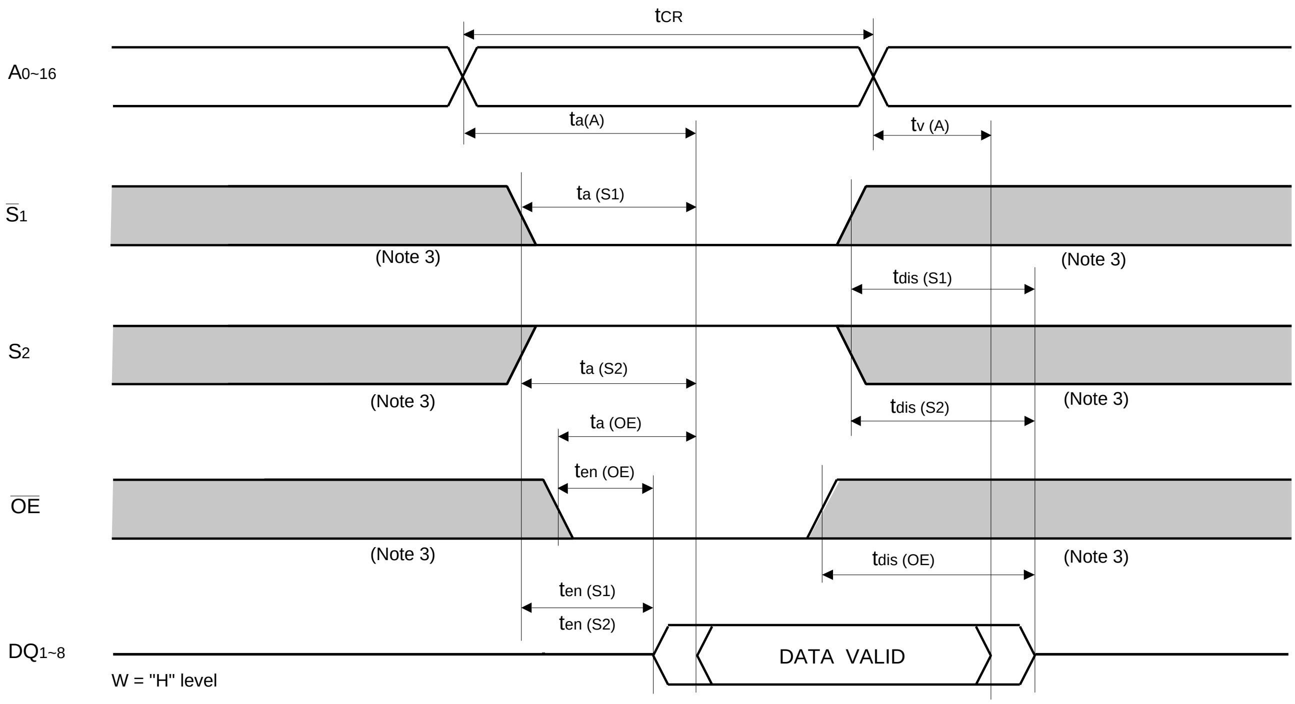
Symbol	Parameter	Limits						Unit
		-55L,LL		-70L,LL		-10L,LL		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		100		ns
$t_{a(A)}$	Address access time		55		70		100	ns
$t_{a(S1)}$	Chip select 1 access time		55		70		100	ns
$t_{a(S2)}$	Chip select 2 access time		55		70		100	ns
$t_{a(OE)}$	Output enable access time		30		35		50	ns
$t_{dis(S1)}$	Output disable time after $\overline{S}_1$ high		20		25		35	ns
$t_{dis(S2)}$	Output disable time after S_2 low		20		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		35	ns
$t_{en(S1)}$	Output enable time after $\overline{S}_1$ low	5		10		10		ns
$t_{en(S2)}$	Output enable time after S_2 high	5		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns
$t_{V(A)}$	Data valid time after address	5		10		10		ns

(3) WRITE CYCLE

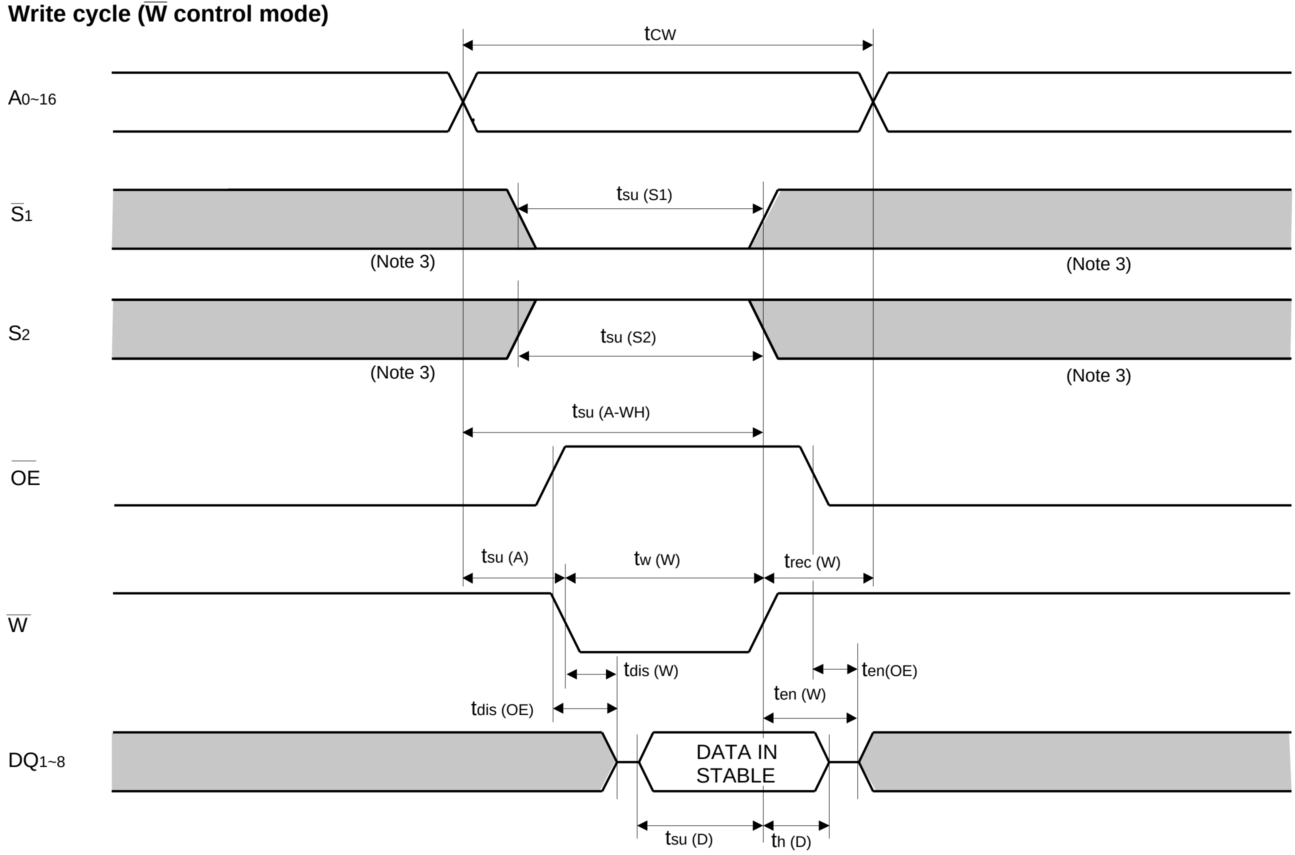
Symbol	Parameter	Limits						Unit
		-55L,LL		-70L,LL		-10L,LL		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		100		ns
$t_{w(W)}$	Write pulse width	45		55		75		ns
$t_{su(A)}$	Address setup time	0		0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to $\overline{W}$	50		65		85		ns
$t_{su(S1)}$	Chip select 1 setup time	50		65		85		ns
$t_{su(S2)}$	Chip select 2 setup time	50		65		85		ns
$t_{su(D)}$	Data setup time	25		30		40		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		20		25		35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		20		25		35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		ns

(4) TIMING DIAGRAMS

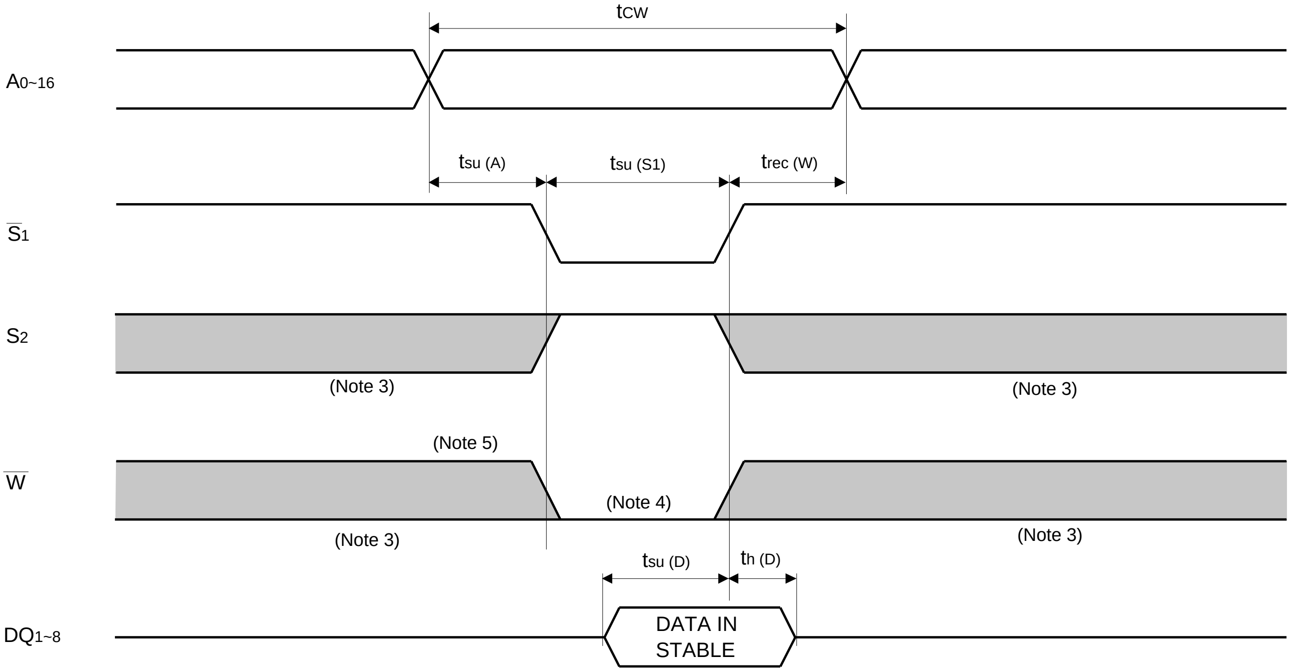
Read cycle



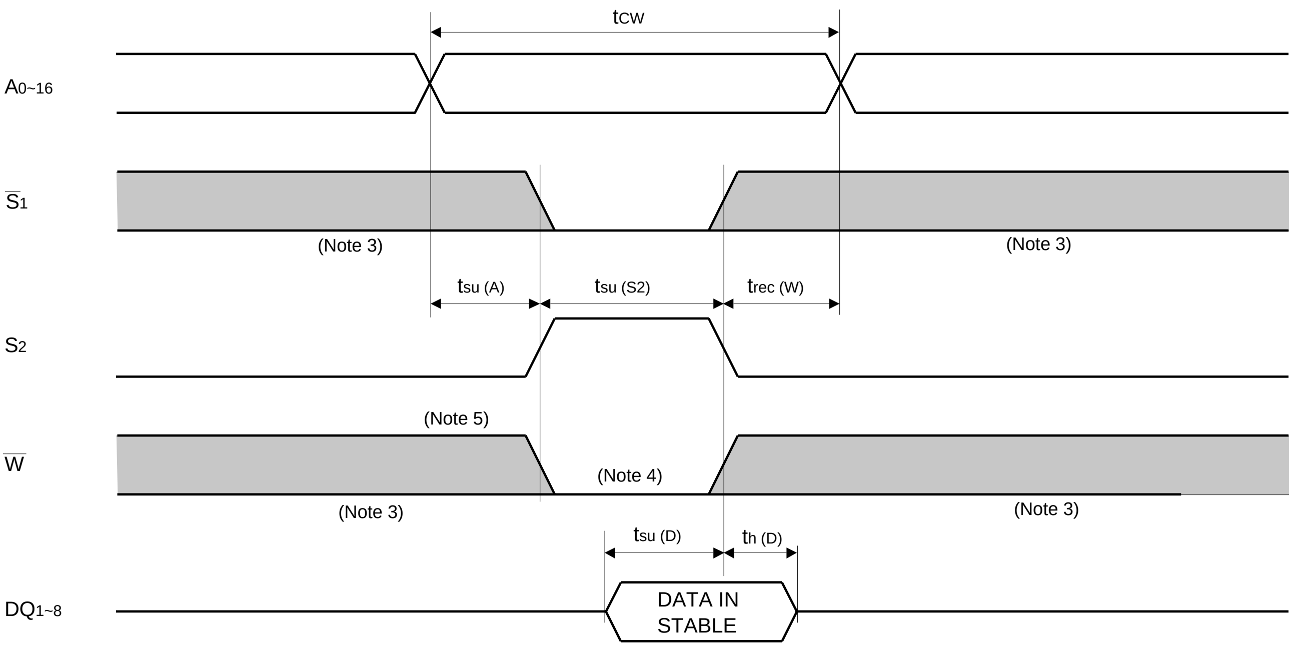
Write cycle (W control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S2 control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while S_2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}_1$ or rising edge of S_2, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\,(PD)}$	Power down supply voltage			2			V
$V_{I\,(S1)}$	Chip select input $\overline{S}_1$	2.2V ≤ Vcc(PD)		2.2			V
		2V ≤ Vcc(PD) ≤2.2V			Vcc(PD)		
$V_{I\,(S2)}$	Chip select input S_2	4.5V ≤ Vcc(PD)				0.8	V
		Vcc(PD) < 4.5V				0.2	
$I_{CC\,(PD)}$	Power down supply current	V_{CC} = 3V 1) S_2 ≤ 0.2V, other inputs = 0~3V 2) $\overline{S}_1$ ≥ V_{CC} - 0.2V,S_2 ≥ V_{CC} - 0.2V other inputs = 0~3V	-L			50	µA
			-LL		0.3	10 (Note 7)	

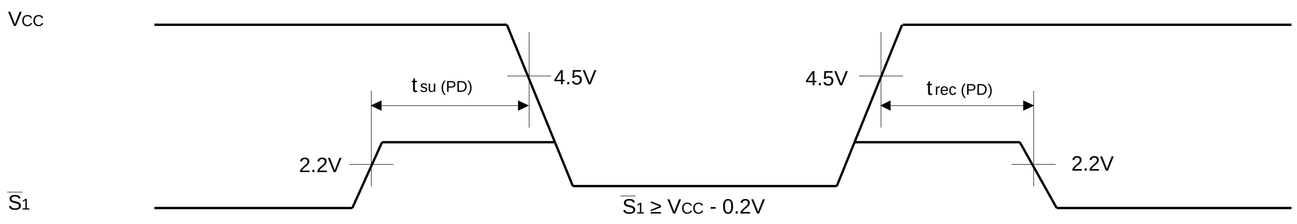
Note7: $I_{CC\,(PD)}$ = 1µA in case of Ta = 25°C

(2) TIMING REQUIREMENTS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\,(PD)}$	Power down set up time		0			ns
$t_{rec\,(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S}_1$ control mode



S_2 control mode