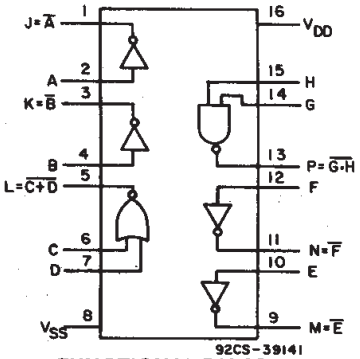
TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS090C − Revised October 2003

# CD4572UB Types




FUNCTIONAL DIAGRAM

## CMOS Hex Gate

Four Inverters, One 2-Input NOR Gate, One 2-Input NAND Gate

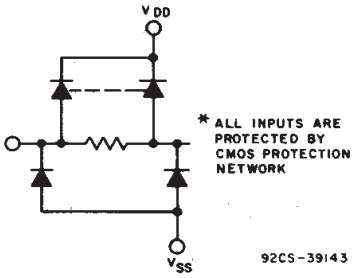
**Features:**

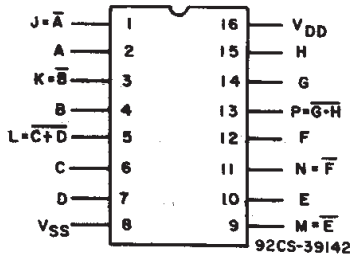
- *Pin 7 NOR input positioned adjacent to $V_{SS}$ for easy use of gate as an inverter*
- *Pin 15 NAND input positioned adjacent to $V_{DD}$ for easy use of gate as an inverter*
- *Standard symmetrical output characteristics*
- *100% tested for quiescent current at 20 V*
- *Maximum input current of 1 μA at 18 V over full package-temperature range: 100 nA at 18 V and 25° C*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*

■ CD4572UB Hex Gate provides the system designer with direct implementation of inverter, NAND, and NOR functions and supplements the existing family of CMOS gates.

The CD4572UB devices meet all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

The CD4572UB types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).




TERMINAL ASSIGNMENT

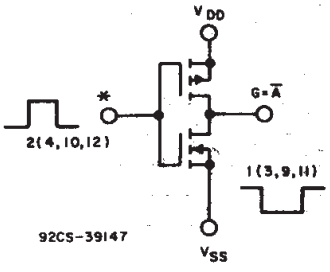



Fig. 1 - Schematic diagram of one of four identical inverters.

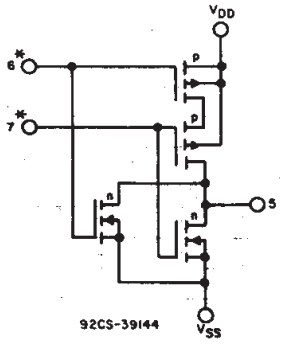



Fig. 2 - Schematic diagram for the 2-input NOR gate.

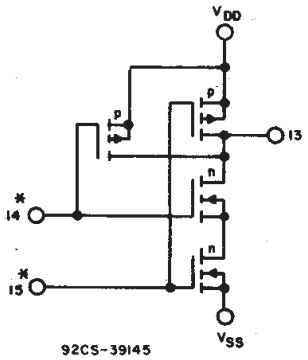



Fig. 3 - Schematic diagram for the 2-input NAND gate.

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

## RECOMMENDED OPERATING CONDITIONS

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| Supply-Voltage Range (For $T_A$=Full Package-Temperature Range) | 3 | 18 | V |

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | | | | | +25 | | | |
| | | | | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | — | 0, 5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | — | 0.01 | 0.25 | μA |
| | — | 0, 10 | 10 | 0.5 | 0.5 | 15 | 15 | — | 0.01 | 0.5 | |
| | — | 0, 15 | 15 | 1 | 1 | 30 | 30 | — | 0.01 | 1 | |
| | — | 0, 20 | 20 | 5 | 5 | 150 | 150 | — | 0.02 | 5 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0, 5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA |
| | 0.5 | 0, 10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| | 1.5 | 0, 15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0, 5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | |
| | 2.5 | 0, 5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | |
| | 9.5 | 0, 10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| | 13.5 | 0, 15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | — | 0, 5 | 5 | 0.05 | | | | — | 0 | 0.05 | V |
| | — | 0, 10 | 10 | 0.05 | | | | — | 0 | 0.05 | |
| | — | 0, 15 | 15 | 0.05 | | | | — | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | — | 0, 5 | 5 | 4.95 | | | | 4.95 | 5 | — | |
| | — | 0, 10 | 10 | 9.95 | | | | 9.95 | 10 | — | |
| | — | 0, 15 | 15 | 14.95 | | | | 14.95 | 15 | — | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5, 4.5 | — | 5 | 1 | | | | — | — | 1 | |
| | 1, 9 | — | 10 | 2 | | | | — | — | 2 | |
| | 1.5, 13.5 | — | 15 | 2.5 | | | | — | — | 2.5 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5, 4.5 | — | 5 | 4 | | | | 4 | — | — | |
| | 1, 9 | — | 10 | 8 | | | | 8 | — | — | |
| | 1.5, 13.5 | — | 15 | 12.5 | | | | 12.5 | — | — | |
| Input Current, $I_{IN}$ Max. | — | 0, 18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | $\pm 10^{-5}$ | ±0.1 | μA |

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$=25°C, Input $t_r$,$t_f$=20 ns, $C_L$=50 pF, $R_L$=200 KΩ**

| CHARACTERISTIC | SYMBOL | TEST CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|
| | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| Propagation Delay Time | $t_{PHL}$, $t_{PLH}$ | 5 | — | 100 | 200 | ns |
| | | 10 | — | 55 | 110 | |
| | | 15 | — | 40 | 85 | |
| Transition Time | $t_{THL}$, $t_{TLH}$ | 5 | — | 100 | 200 | |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Input Capacitance | $C_{IN}$ | Any Input | — | 10 | 15 | pF |

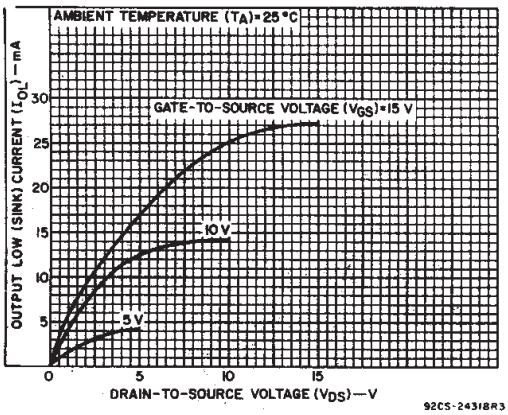



*Fig. 4 - Typical output low (sink) current characteristics.*

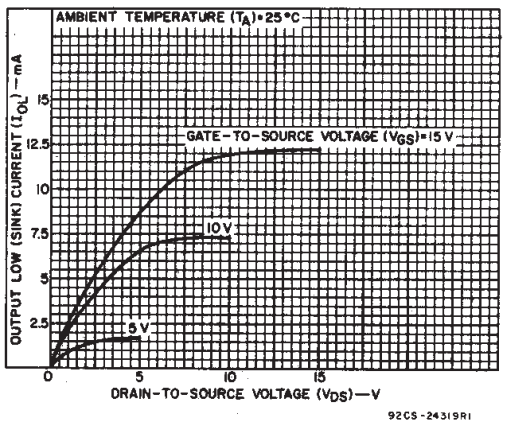



*Fig. 5 - Minimum output low (sink) current characteristics.*

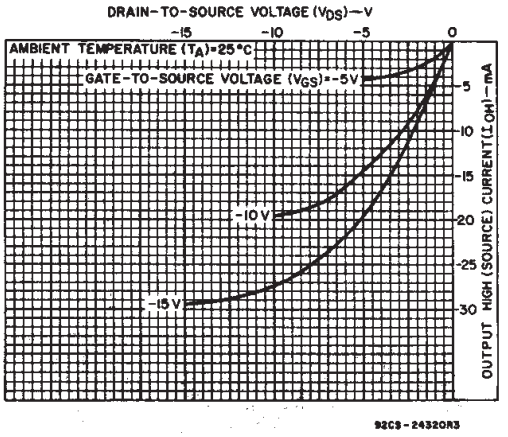



*Fig. 6 - Typical output high (source) current characteristics.*

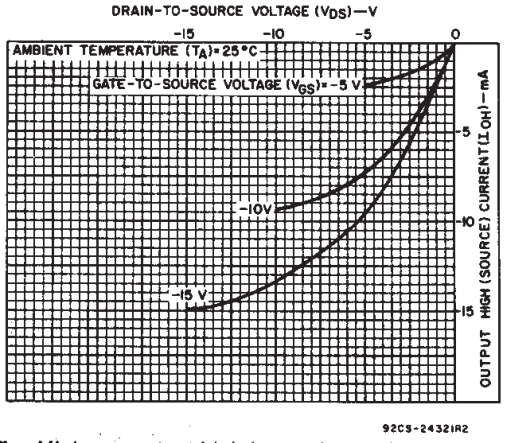



*Fig. 7 - Minimum output high (source) current characteristics.*

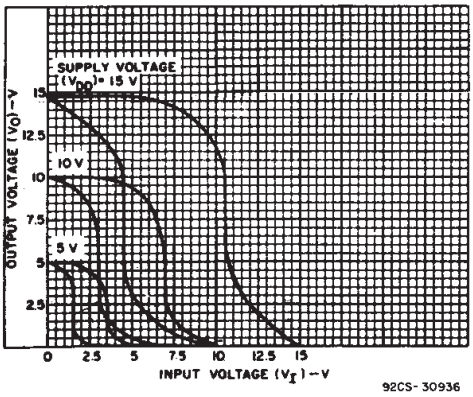



*Fig. 8 - Minimum and maximum inverter voltage transfer characteristics.*

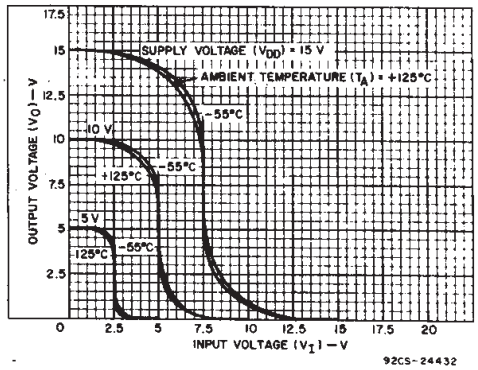



*Fig. 9 - Typical inverter voltage transfer characteristics as a function of temperature.*

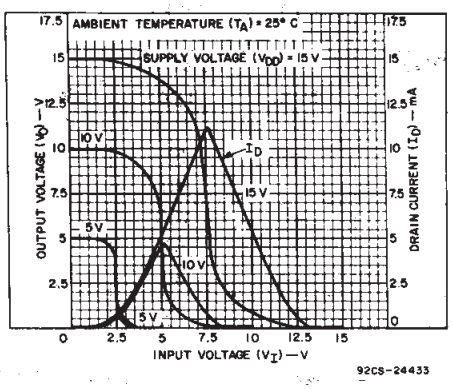



Fig. 10 - Typical inverter current and voltage transfer characteristics.

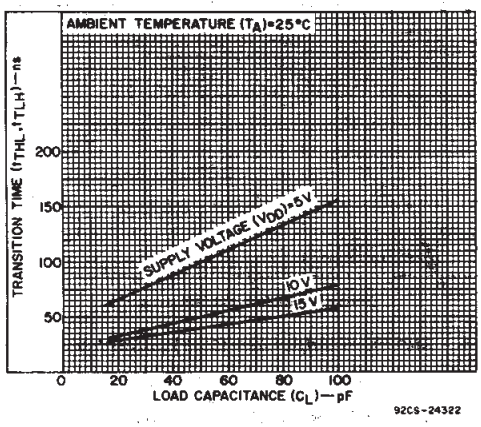



Fig. 12 - Typical transition time vs. load capacitance.

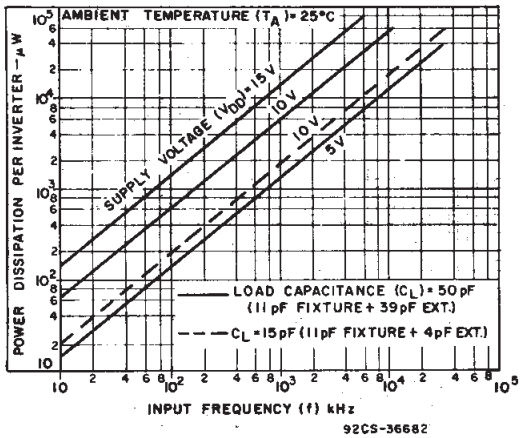



Fig. 14 - Typical dynamic power dissipation vs. frequency.

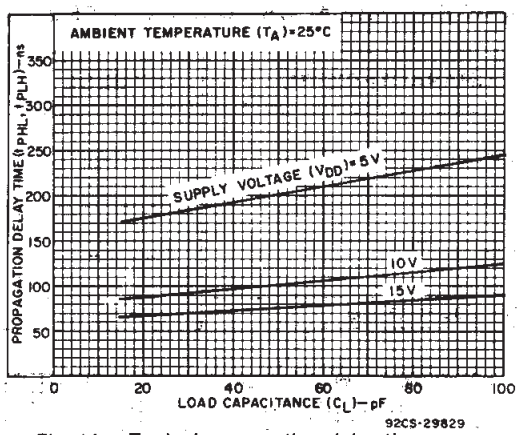



Fig. 11 - Typical propagation delay time as a function of load capacitance.

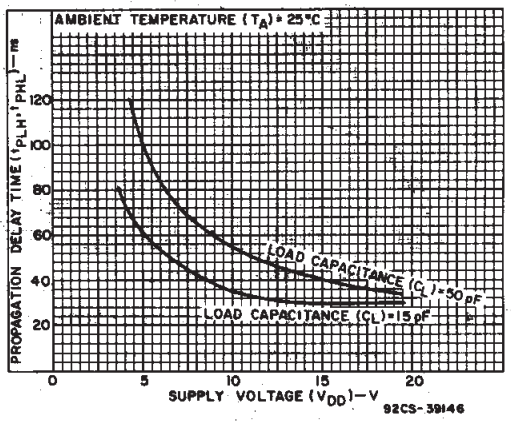



Fig. 13 - Typical propagation delay time vs. supply voltage.

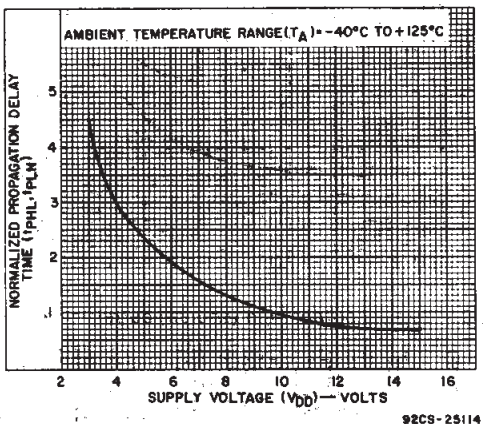



Fig. 15 - Variation of normalized propagation delay time ($t_{PHL}$ and $t_{PLH}$) with supply voltage.

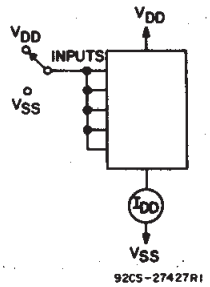



Fig. 16 - Quiescent device current test circuit.

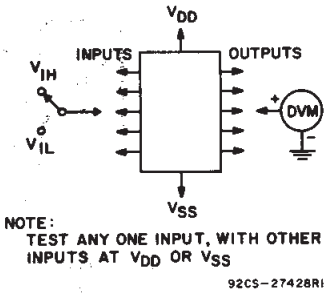



Fig. 17 - Noise immunity test circuit.

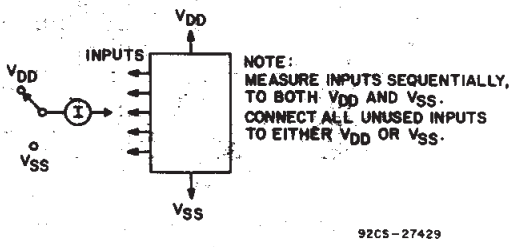



Fig. 18 - Input leakage current test circuit.

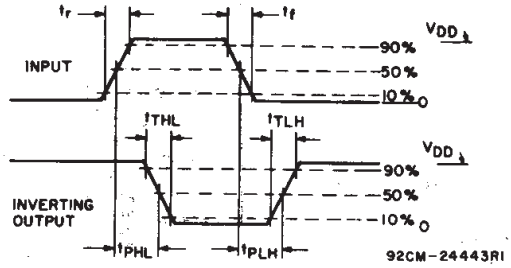
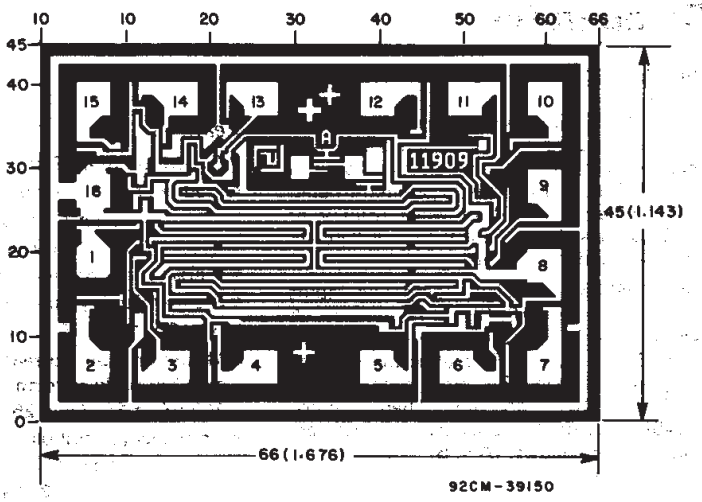



*Fig. 19 - Transition times and propagation delay times, combination logic.*




*Dimensions and pad layout for CD4572UBH.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| CD4572UBE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4572UBEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4572UBM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBM96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBM96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBM96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBMG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBMT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBMTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBMTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4572UBPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

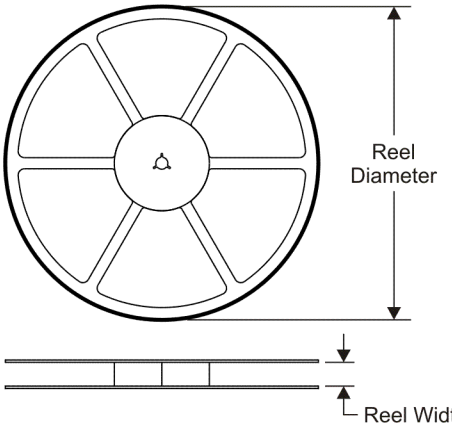
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

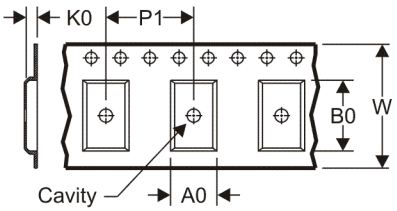
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

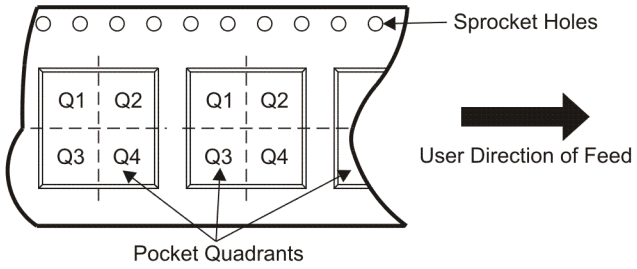



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

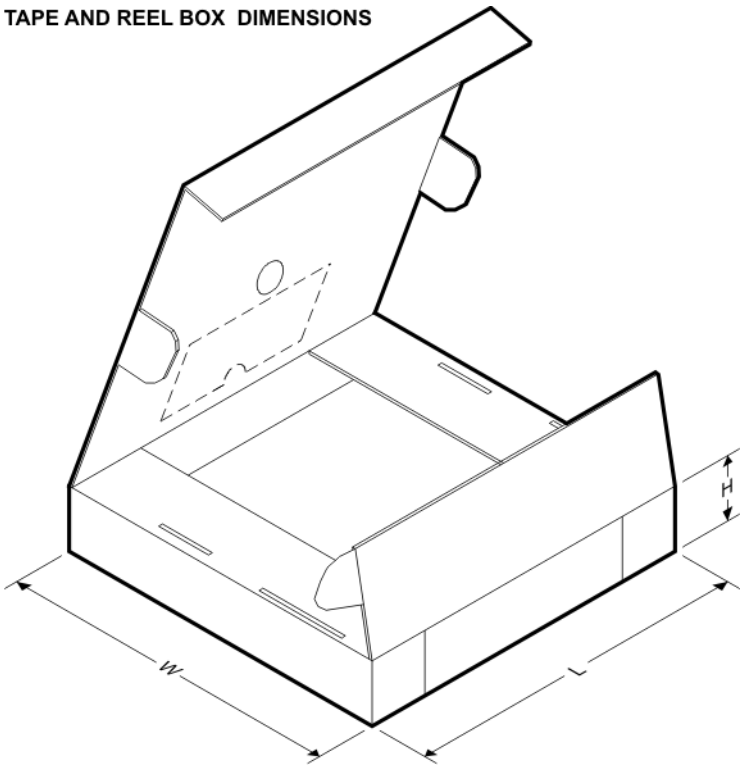
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4572UBM96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4572UBNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4572UBPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



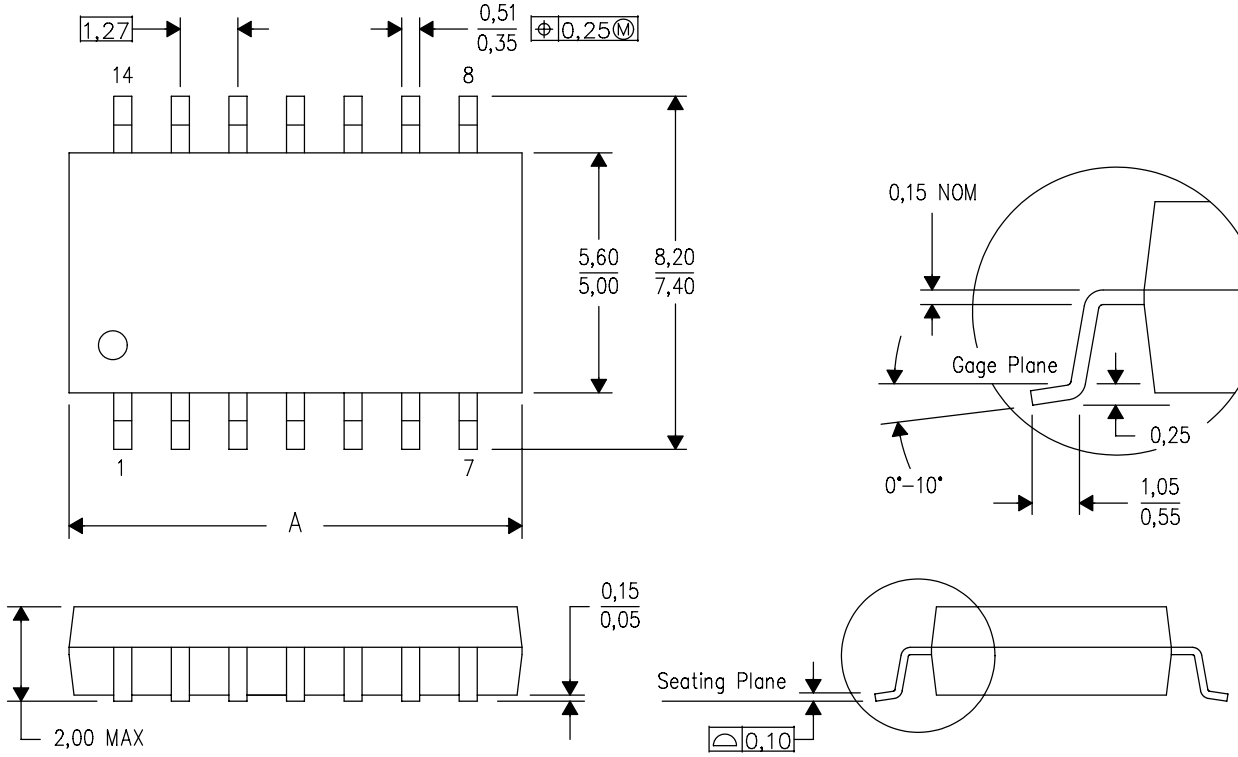

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD4572UBM96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD4572UBNSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| CD4572UBPWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



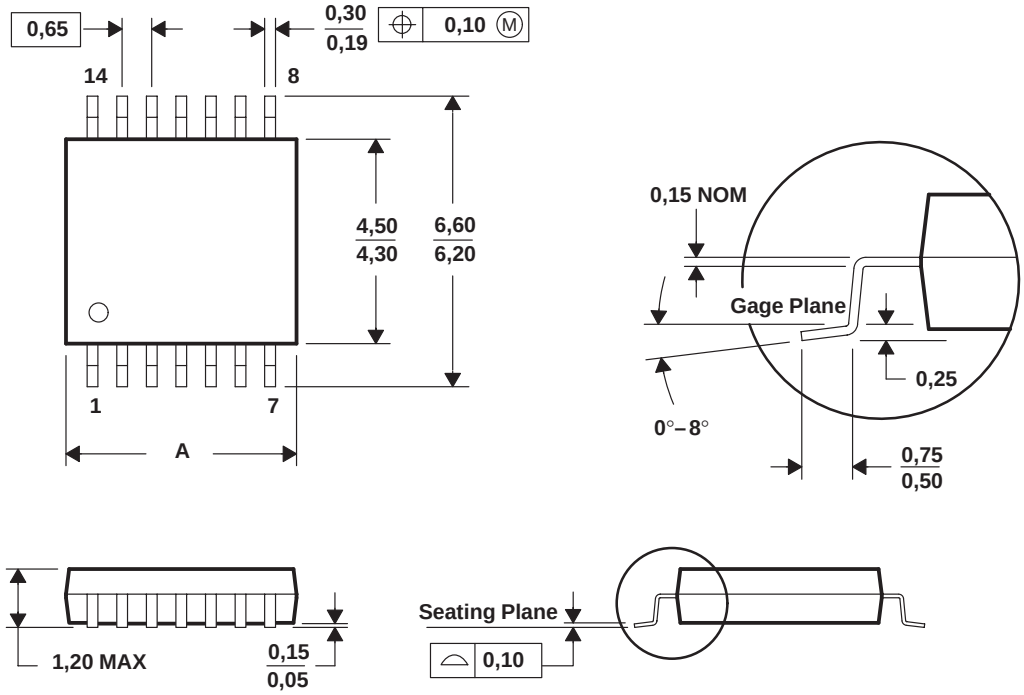

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**

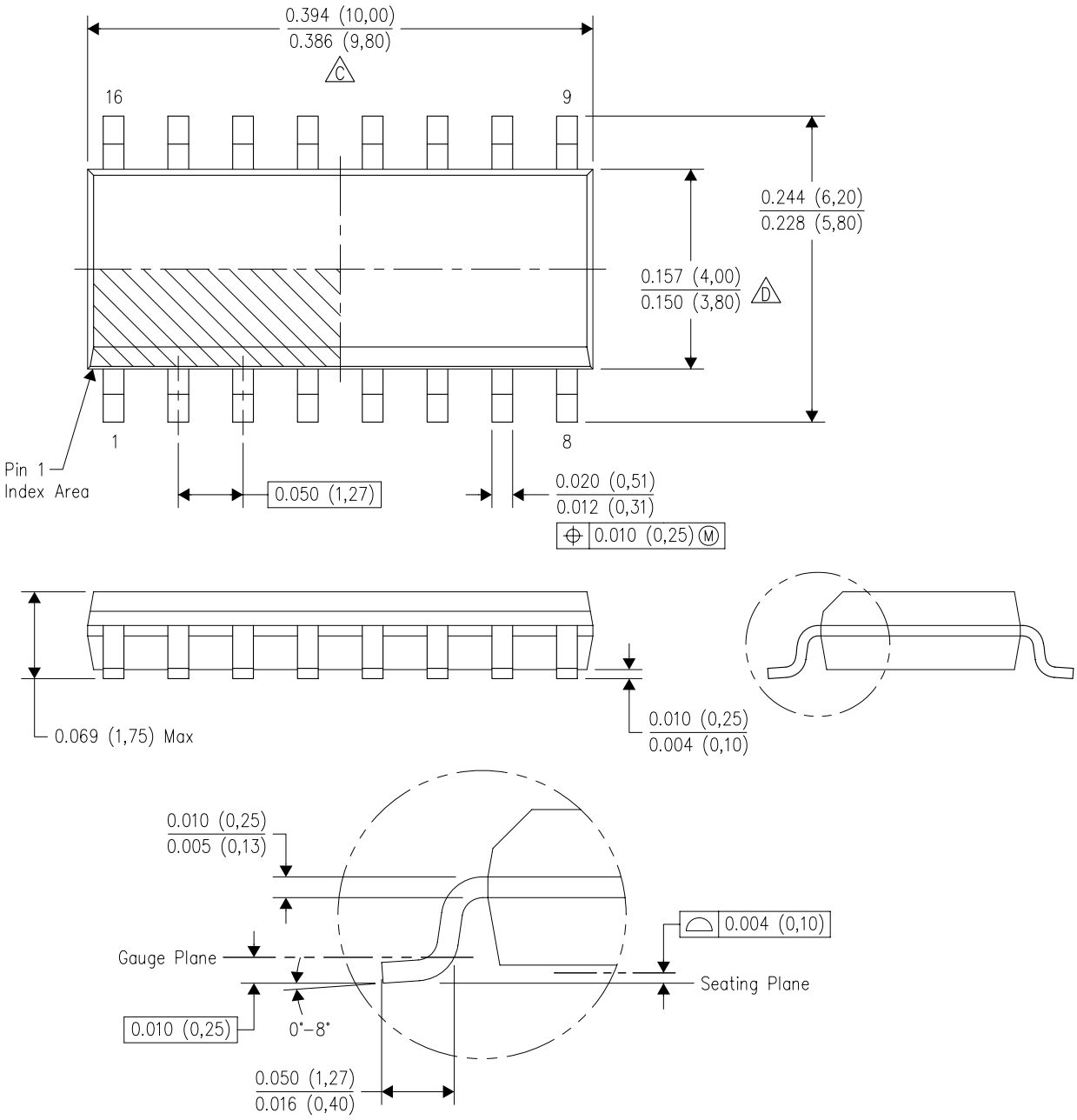



| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

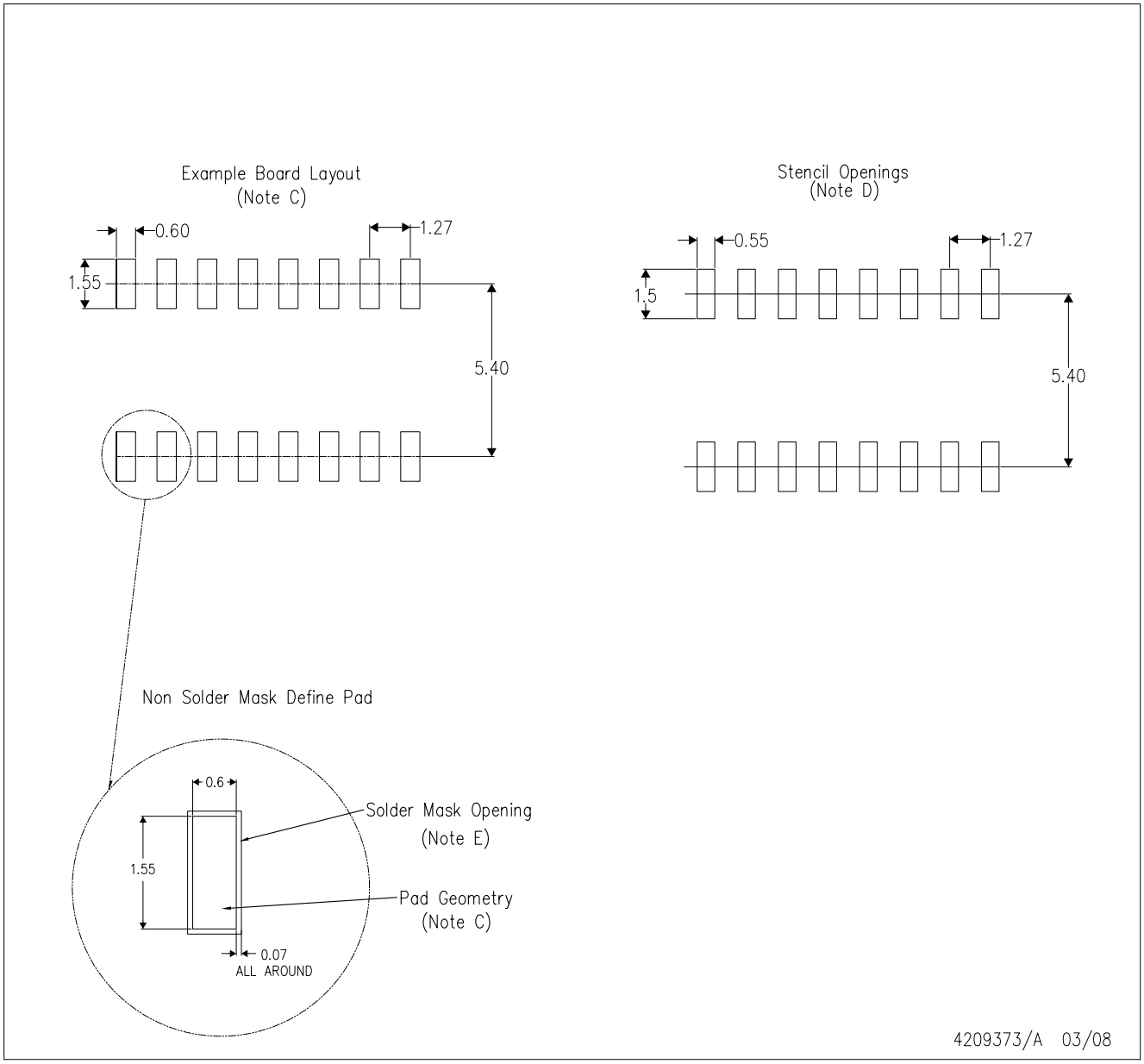
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)

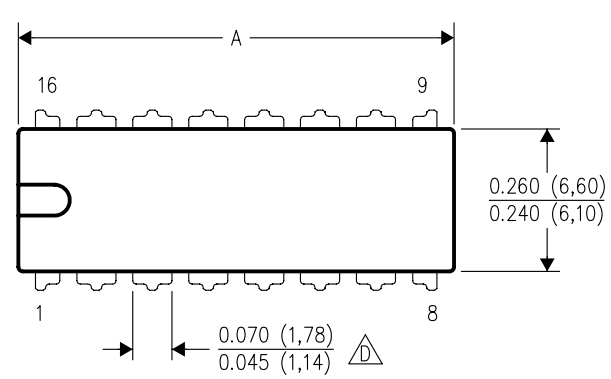



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

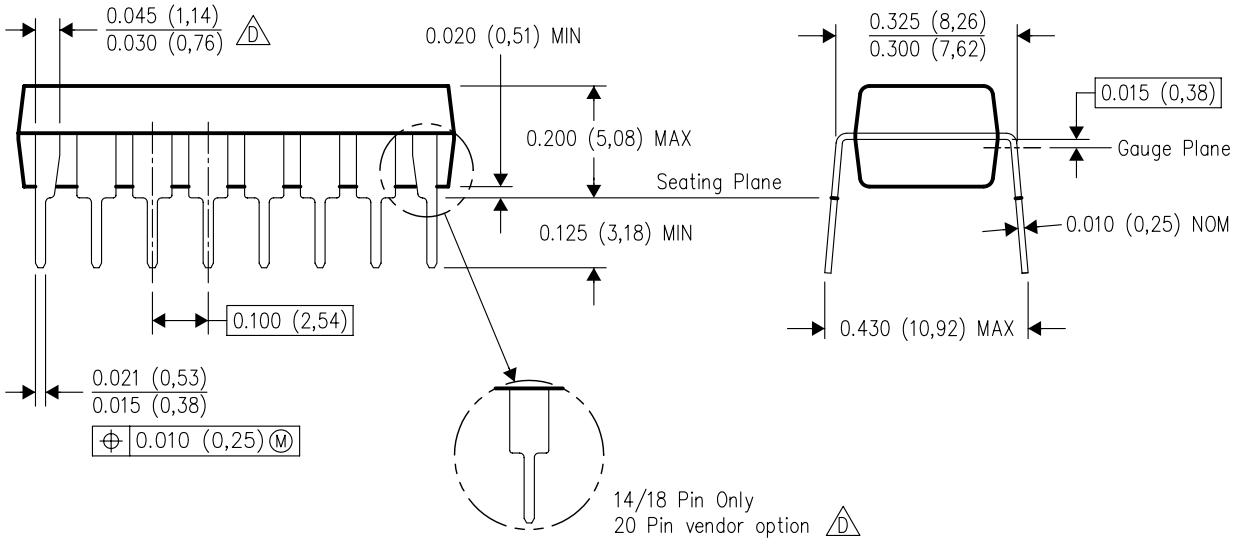
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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