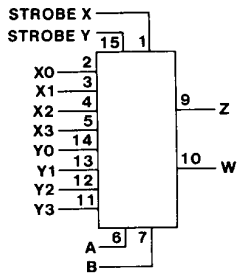
CMOS Logic ICs



FUNCTIONAL DIAGRAM

CMOS Dual 4-Channel Analog Data Selector

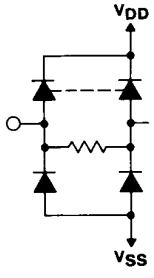
High-Voltage Types (20-Volt Rating)

Features:

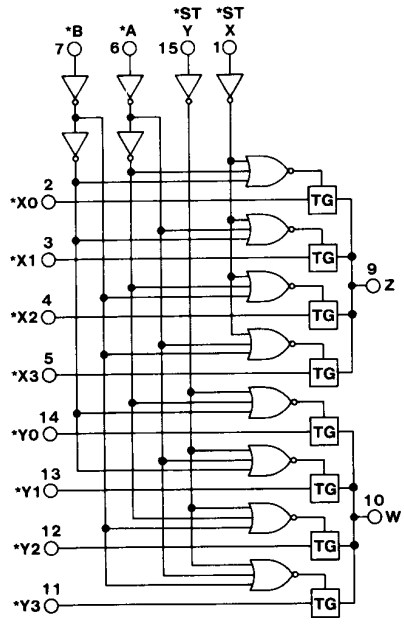
- *Wide range of digital and analog signal levels:*
  Digital: 3 to 20 V
  Analog: 0 to 20 V_{p-p}
- *Low ON-state resistance: 120 Ω typ. at 15 V*
- *Break-Before-Make switching eliminates channel overlap*
- *100% tested for quiescent current at 20 V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25° C*
- *Noise margin (full package-temperature range) = 1 V at V_{DD}=5 V*
  2 V at V_{DD}=10 V
  2.5 V at V_{DD}=15 V
- *Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*

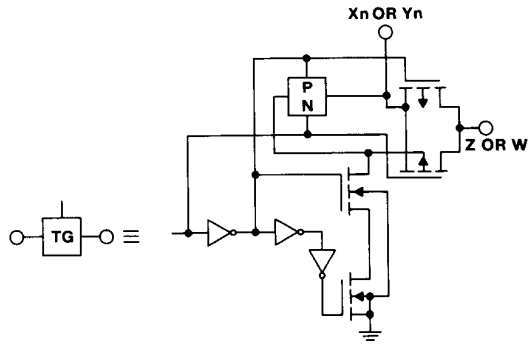
The RCA-CD4529B CMOS dual 4-channel analog data selector consists of digitally controlled analog switches having low on-impedance and very low off-leakage current. The CD4529B is bidirectional and can also be used in digital applications. By tying Z and W together the device can be used as a single 8-channel analog data selector.

The CD4529B device is supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



*ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK.





LOGIC DIAGRAM

92CM-39301

Fig. 1 - Schematic and logic diagram.

Printed in USA/8-85

File Number **1720**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPES D,F,K) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPES D,F,K) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D,F,K,H ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... 265° C

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

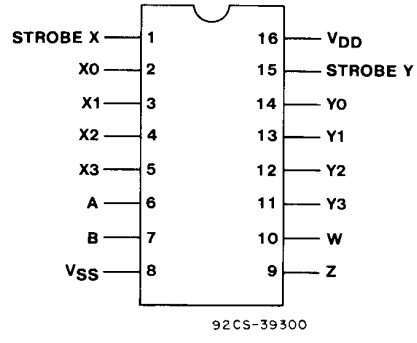
CHARACTERISTIC	V_{DD}	Min.	Max.	UNITS
Supply-Voltage Range (T_A = Full Package-Temperature Range)	—	3	18	V
Multiplexer Switch Input Current Capability*	—	—	25	mA
Output Load Resistance	—	100	—	Ω

* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in Electrical Characteristics Chart). No V_{DD} current will flow through R_L if the switch current flows into terminals 9 and 10 (Z and W, respectively).

TRUTH TABLE

INPUT				OUTPUT		
STROBE X	STROBE Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode (2 Outputs)
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode (1 Output: Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	*	*	High Impedance		

* = Don't Care



TERMINAL ASSIGNMENT

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at -55,+25,+125, apply to D,F,H pkgs Values at -40,+25,+85, apply to E pkg							UNITS
		V_{SS} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
SIGNAL INPUTS (V_{IN}) AND OUTPUTS (V_{OUT})											
Quiescent Device Current, I_{DD} Max.			5	5	5	150	150	—	0.04	5	μA
			10	10	10	300	300	—	0.04	10	
			15	20	20	600	600	—	0.04	20	
			20	100	100	3000	3000	—	0.08	100	
On-State Resistance $0 \leq V_{IN} \leq V_{DD}$ r_{ON} Max.		-5	5	400	410	560	640	—	240	480	Ω
		-7.5	7.5	240	250	350	400	—	135	270	
		0	5	800	850	1200	1300	—	470	1050	
		0	10	400	410	560	640	—	240	480	
		0	15	250	250	350	400	—	135	270	
Change in On-State Resistance (Between Any Two Channels) Δr_{ON}		0	5	—	—	—	—	—	15	—	Ω
		0	10	—	—	—	—	—	10	—	
		0	15	—	—	—	—	—	5	—	
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.		0	18	±100*		±1000*		—	±0.01	±100*	nA
Capacitance: Input, C_{IN}		-5	5	—	—	—	—	—	5	—	pF
Output, C_{OUT}				—	—	—	—	—	18	—	
Feedthrough, C_{IOS}				—	—	—	—	—	0.2	—	
Propagation Delay Time (Signal Input to Output) (t_{PHL}, t_{PLH})	V_{SS}=0, R_L=1 kΩ, C_L=50 pF, V_{IN}=V_{DD}-Vss (Square Wave), t_r,t_f=20 ns	0	5	—	—	—	—	—	20	40	ns
			10	—	—	—	—	—	10	20	
			15	—	—	—	—	—	8	15	
CONTROL (ADDRESS OR STROBE) V_C											
Input Low Voltage, V_{ILC} Max.	V_{IN}=V_{DD}, R_L=1 kΩ to V_{SS} $f_{IS} < 2$ μA on all OFF Channels		5	1.5				—	—	1.5	V
			10	3				—	—	3	
			15	4				—	—	4	
Input High Voltage, V_{IHC} Min.			5	3.5				3.5	—	—	
			10	7				7	—	—	
			15	11				11	—	—	
Input Current, I_{IN} Max.	V_{IN}=0, 18		18	±0.1	±0.1	±1	±1	—	$\pm 10^{-5}$	±0.1	μA
Propagation Delay Time: Control to Signal OUT (t_{PHL}, t_{PLH})	t_r,t_f=20 ns, R_L=1 kΩ, C_L=50 pF, V_{IN}=V_{DD}-Vss (Square Wave)		5	—	—	—	—	—	200	400	ns
			10	—	—	—	—	—	80	160	
			15	—	—	—	—	—	60	120	
Input Capacitance, C_{IN} (Any Address or Strobe Input)			—	—	—	—	—	—	5	7.5	pF

*Determined by minimum feasible leakage measurement for automatic testing.

ELECTRICAL CHARACTERISTICS (Cont'd) at T_A = 25° C

CHARACTERISTIC	TEST CONDITIONS	V_{DD}	LIMITS Min.	Typ.	Max.	UNITS
Crosstalk Voltage, Control to Output	R_L = 1 kΩ, C_L = 50 pF, R_{OUT} = 10 kΩ	5	—	5	—	mV
		10	—	5	—	
		15	—	5	—	
Maximum Control Input Pulse Frequency	R_L = 1 kΩ, C_L = 50 pF	5	—	5	—	MHz
		10	—	10	—	
		15	—	12	—	
Noise Voltage	f = 100 Hz	5	—	24	—	$\frac{nV}{\sqrt{cycle}}$
		10	—	25	—	
		15	—	30	—	
	f = 100 kHz	5	—	12	—	
		10	—	12	—	
		15	—	15	—	
Sine Wave Distortion	V_{IN} = 1.77 V dc (RMS) centered at 0 V dc, R_L = 10 kΩ, f = 1 kHz, V_{SS} = -5 V	5	—	0.36	—	%
Insertion Loss	V_{IN} = 1.77 V dc (RMS) centered at 0 V dc, f = 1 MHz, V_{SS} = -5 V, $I_{Loss} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$					
	R = 1 kΩ	5	—	2	—	dB
	R = 10 kΩ		—	0.8	—	
	R = 100 kΩ		—	0.25	—	
	R = 1 MΩ		—	0.01	—	
Bandwidth (-3 dB)	V_{IN} = 1.77 V dc (RMS) centered at 0 V dc, V_{SS} = -5 V					
	R = 1 kΩ	5	—	35	—	MHz
	R = 10 kΩ		—	28	—	
	R = 100 kΩ		—	27	—	
	R = 1 MΩ		—	26	—	
Feedthrough and Crosstalk	V_{SS} = -5 V, $20 \log_{10} \frac{V_{OUT}}{V_{IN}}$ = -50 dB					
	R = 1 kΩ	5	—	850	—	kHz
	R = 10 kΩ		—	100	—	
	R = 100 kΩ		—	12	—	
	R = 1 MΩ		—	1.5	—	

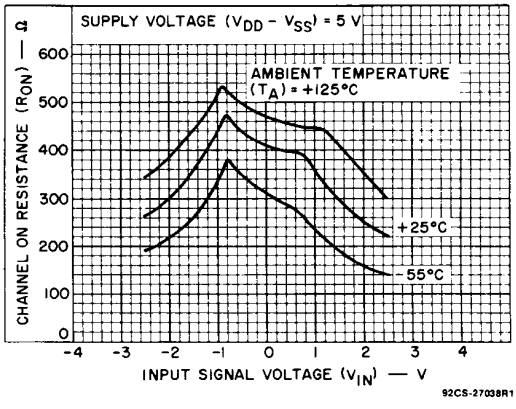


Fig. 2 - Typical channel ON resistance vs. input signal voltage.

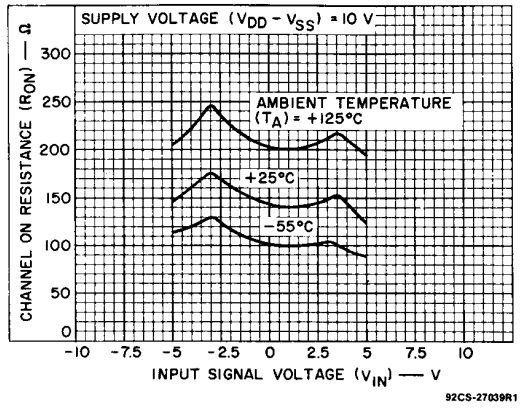


Fig. 3 - Typical channel ON resistance vs. input signal voltage.

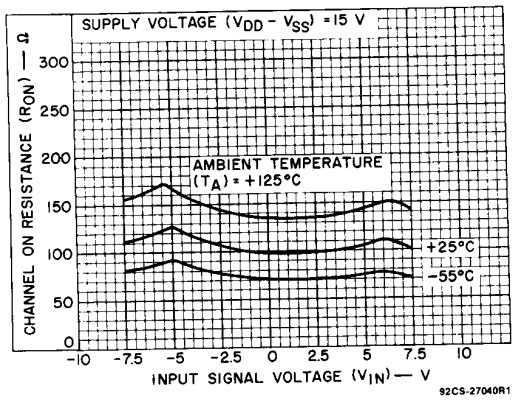


Fig. 4 - Typical channel ON resistance vs. input signal voltage.

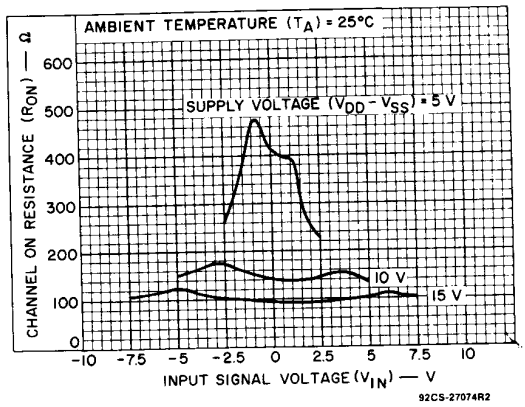


Fig. 5 - Typical channel ON resistance vs. input signal voltage.

TEST CIRCUITS

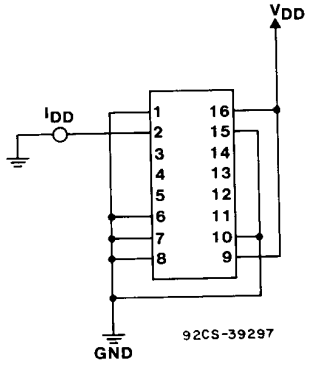


Fig. 6 - OFF channel leakage current- any channel OFF.

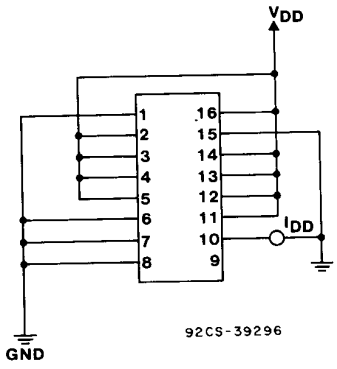


Fig. 7 - OFF channel leakage current, all channels OFF.

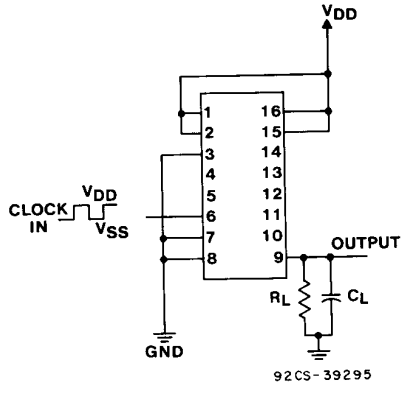


Fig. 8 - Propagation delay address input to signal output.

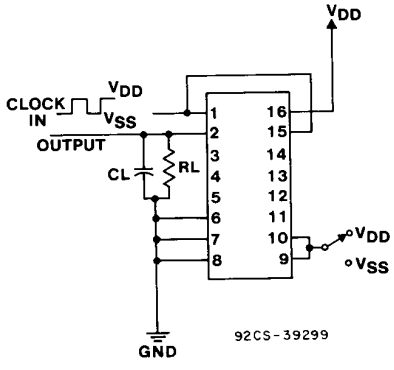


Fig. 9 - Propagation delay-strobe input to signal output.

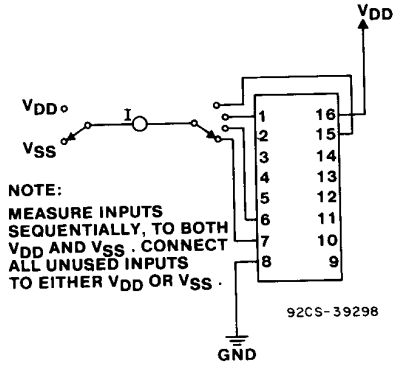


Fig. 10 - Quiescent device current.

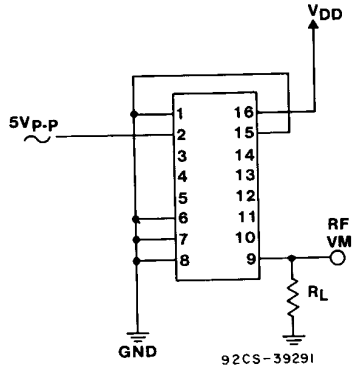


Fig. 11 - Feedthrough.

TEST CIRCUITS (Cont'd)

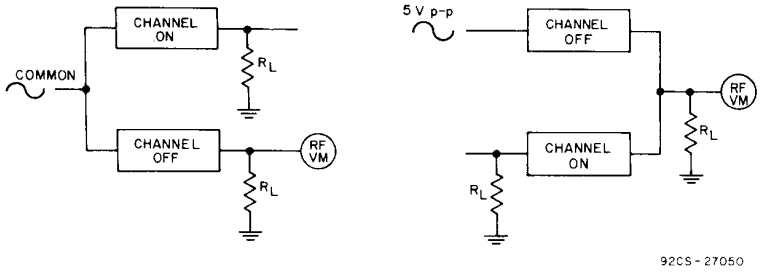


Fig. 12 - Crosstalk between any two channels.

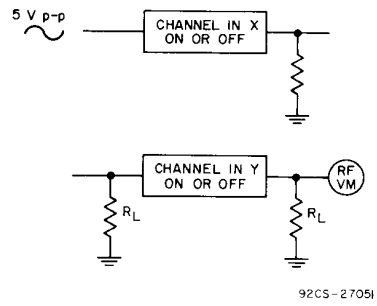


Fig. 13 - Crosstalk between sections.

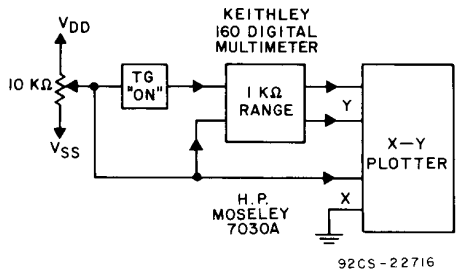
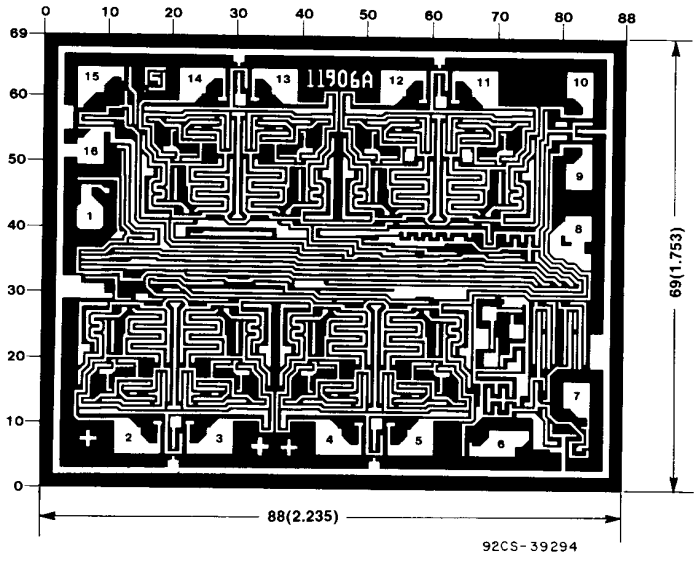


Fig. 14 - Channel ON resistance measurement circuit.



Dimensions and pad layout for CD4529B.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +10 mils applicable to the nominal dimensions shown.

Dimensions in parenthese are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

ORDERING INFORMATION

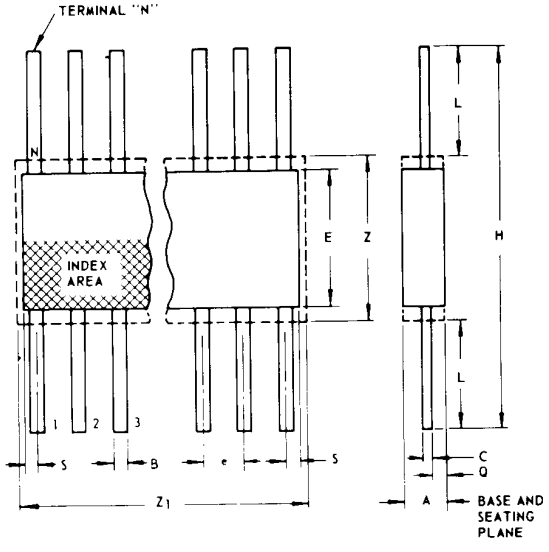
RCA CMOS device packages are identified by suffix letters indicated in the following chart. When ordering a CMOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-in-Line Welded-Seal Ceramic	D
Dual-in-Line Plastic	E
Dual-In-Line Frit-Seal Ceramic	F
Chip	H
Ceramic Flat Pack	K

For example, a CDP4529B in a dual-in-line plastic package will be identified as the CDP4529BE.

DIMENSIONAL OUTLINES

Ceramic Flat Pack



K SUFFIX
(JEDEC MO-004-AG)
16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

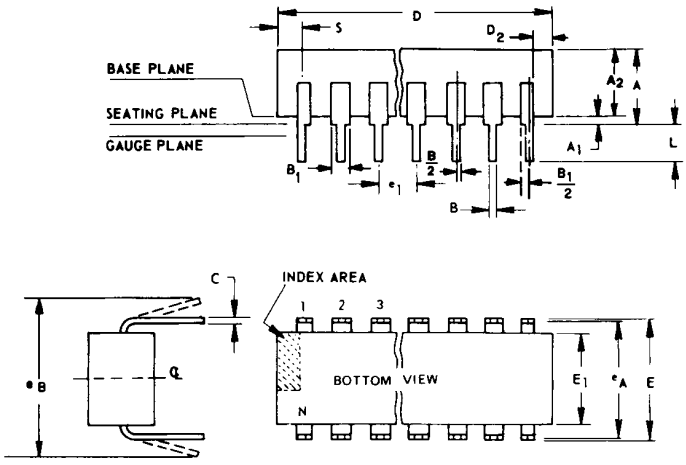
92CS-17271R3

NOTES:

1. Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

DIMENSIONAL OUTLINES (Cont'd)

E AND F SUFFIXES
JEDEC MS-001-AC 16-Lead Dual-In-Line
Plastic or Frit-Seal Ceramic Package



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0^o	15^o	4	0^o	15^o
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	—	0.210	10	—	5.33
A_1	0.015	—	10	0.39	—
A_2	0.115	0.195		2.93	4.95
B	0.014	0.022		0.356	0.558
B_1	0.045	0.070	3	1.15	1.77
C	0.008	0.015		0.204	0.381
D	0.745	0.840	4	18.93	21.33
D_2	0.005	—	5	0.13	—
E	0.300	0.325	6	7.62	8.25
E_1	0.240	0.280	7, 8	6.10	7.11
e_1	0.090	0.110	9	2.29	2.79
e_A	0.300 TP		10	7.62 TP	
e_B	—	0.410	11	—	10.41
L	0.115	0.150	10	2.93	3.81
N	16		12	16	
S	—	—	13	—	—

92CM-34834R1

NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices," Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.