MOTOROLA

SN54/74LS540
SN54/74LS541

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

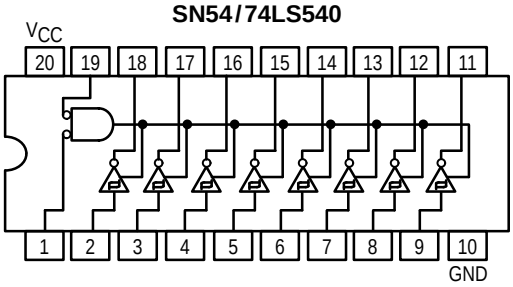
The SN54/74LS540 and SN54/74LS541 are octal buffers and line drivers with the same functions as the LS240 and LS241, but with pinouts on the opposite side of the package.

These device types are designed to be used as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These devices are especially useful as output ports for the microprocessors, allowing ease of layout and greater PC board density.

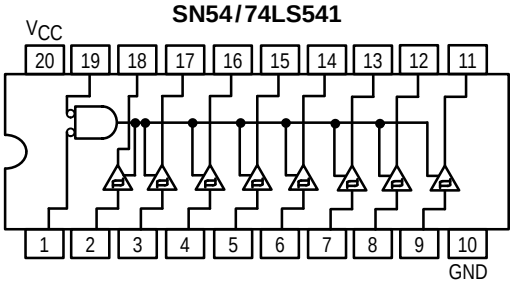
- Hysteresis at Inputs to Improve Noise Margin
- PNP Inputs Reduce Loading
- 3-State Outputs Drive Bus Lines
- Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors
- Input Clamp Diodes Limit High-Speed Termination Effects

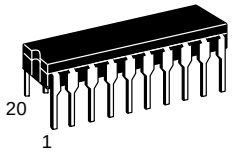
LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)

SN54/74LS540

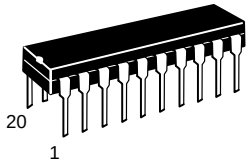


SN54/74LS541

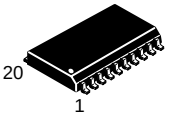




J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

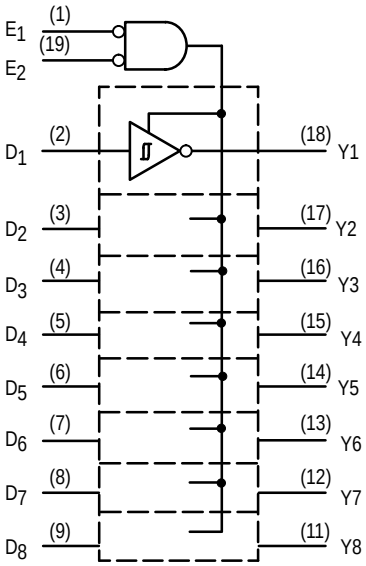
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC

GUARANTEED OPERATING RANGES

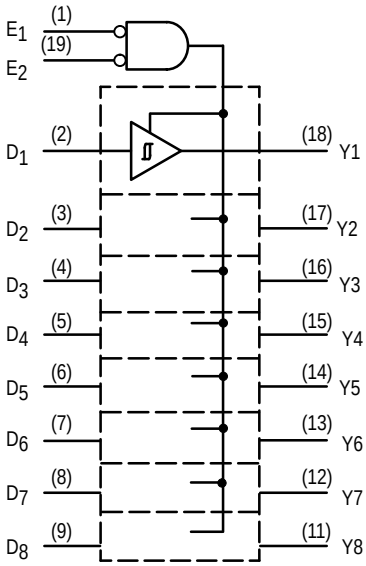
Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			–12 –15	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

BLOCK DIAGRAM

LS540



LS541



INPUTS			OUTPUTS	
E_1	E_2	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA	
		54, 74	2.0			V	V_{CC} = MIN, I_{OH} = MAX, V_{IL} = 0.5 V	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
V_{T+}–V_{T-}	Hysteresis		0.2	0.4		V	V_{CC} = MIN	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−40		−225	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH	LS540			25	mA	V_{CC} = MAX	
		LS541			32	mA		
	Total, Output LOW	LS540			45	mA		
		LS541			52	mA		
	Total Output 3-State	LS540			52	mA		
		LS541			55	mA		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Propagation Delay, Data to Output	LS540		9.0	15	ns	V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω
t_{PLH}		LS541		12	15		
t_{PHL}		LS540		12	15		
t_{PHL}		LS541		12	18		
t_{PZH}	Output Enable Time to HIGH Level	LS540		15	25	ns	
		LS541		15	32		
t_{PZL}	Output Enable Time to LOW Level	LS540		20	38	ns	
		LS541		20	38		
t_{PHZ}	Output Disable Time to HIGH Level	LS540		10	18	ns	C_L = 5.0 pF
		LS541		10	18		
t_{PLZ}	Output Disable Time to LOW Level	LS540		15	25	ns	
		LS541		15	29		

AC WAVEFORMS

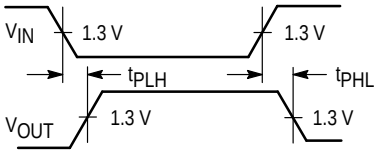


Figure 1

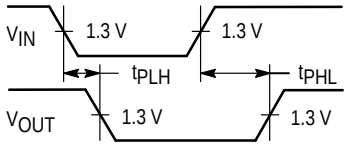


Figure 2

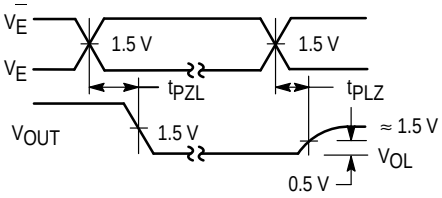


Figure 3

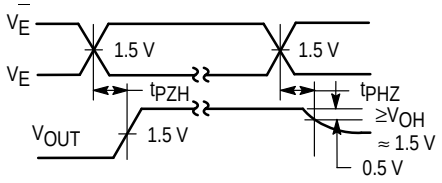
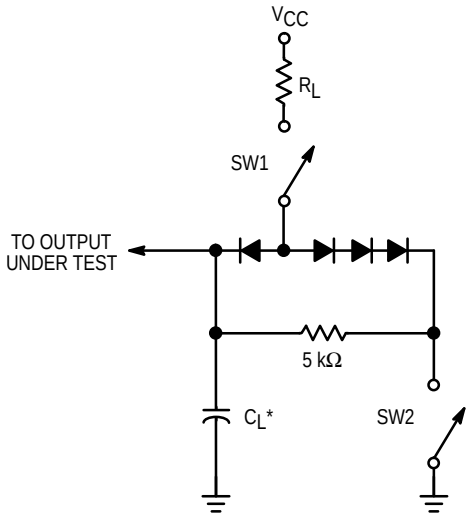


Figure 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 5