SN74LS257B SN74LS258B

Quad 2-Input Multiplexer with 3-State Outputs

The LSTTL/MSI SN74LS257B and the SN74LS258B are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (E_O) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process For High Speed
- Multiplexer Expansion By Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–2.6	mA
I_{OL}	Output Current – Low			24	mA

ON Semiconductor
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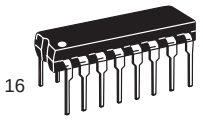
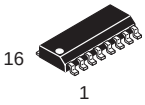
http://onsemi.com

LOW POWER SCHOTTKY



PLASTIC
N SUFFIX
CASE 648

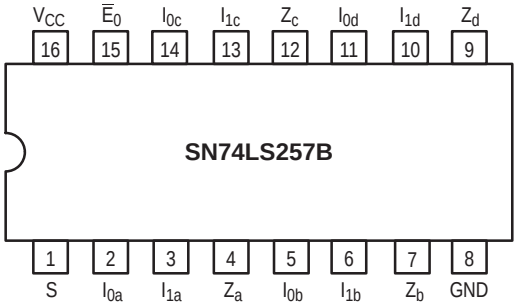


SOIC
D SUFFIX
CASE 751B

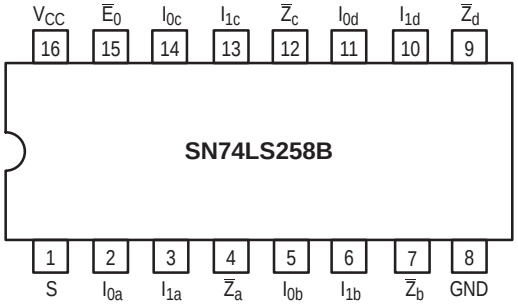
ORDERING INFORMATION

Device	Package	Shipping
SN74LS257BN	16 Pin DIP	2000 Units/Box
SN74LS257BD	16 Pin	2500/Tape & Reel
SN74LS258BN	16 Pin DIP	2000 Units/Box
SN74LS258BD	16 Pin	2500/Tape & Reel

CONNECTION DIAGRAM DIP (TOP VIEW)



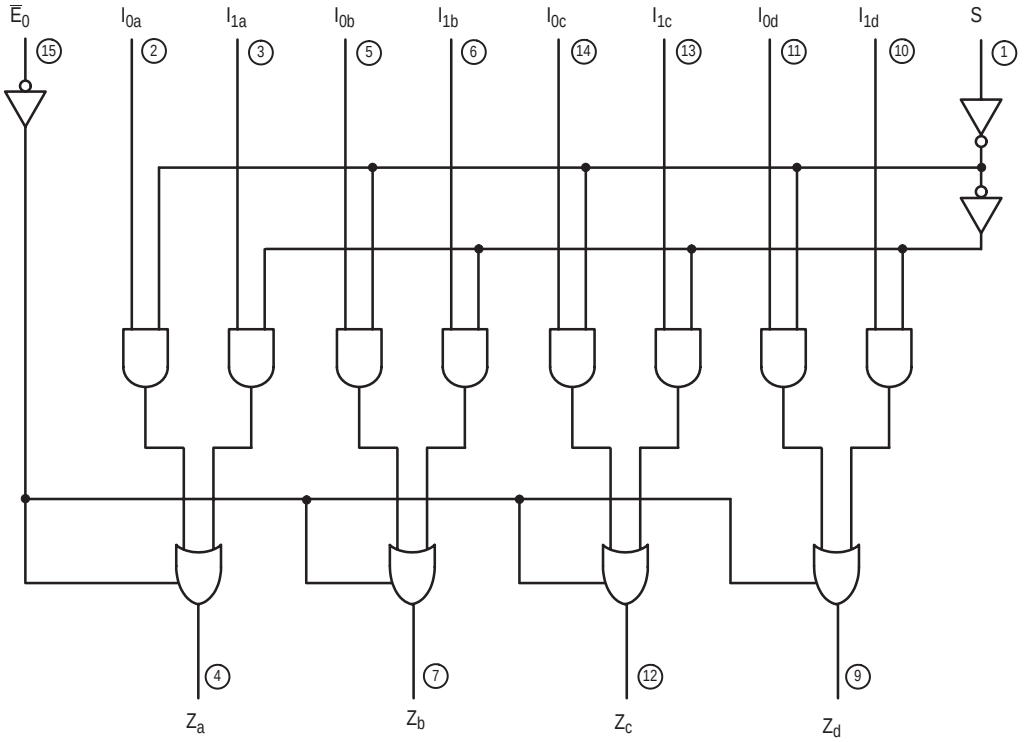
V_{CC} = PIN 16
GND = PIN 8



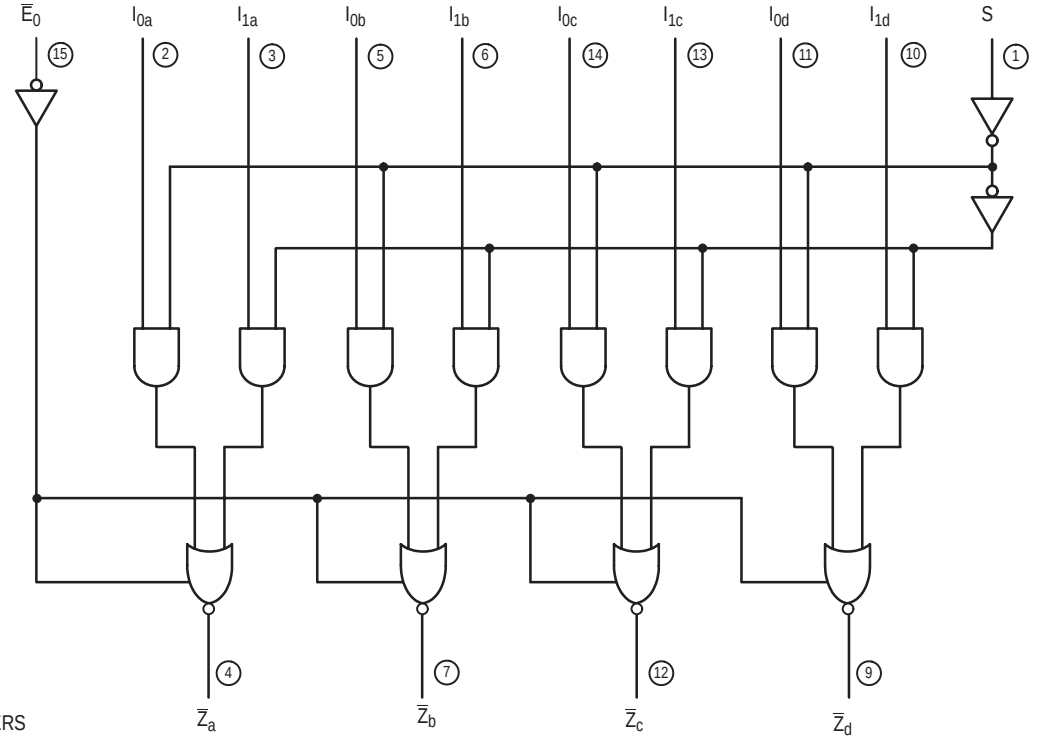
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAMS

SN74LS257B



SN74LS258B



V_{CC} = PIN 16
GND = PIN 8
◯ = PIN NUMBERS

FUNCTIONAL DESCRIPTION

The LS257B and LS258B are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257B and in the inverted form for the LS258B.

The LS257B and LS258B are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

When the Output Enable Input ($\overline{E}_0$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LS257B

$Z_a = \overline{E}_0 \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$ $Z_b = \overline{E}_0 \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$
$Z_c = \overline{E}_0 \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$ $Z_d = \overline{E}_0 \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

LS258B

$\overline{Z}_a = \overline{E}_0 \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$ $\overline{Z}_b = \overline{E}_0 \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$
$\overline{Z}_c = \overline{E}_0 \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$ $\overline{Z}_d = \overline{E}_0 \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS LS257B	OUTPUTS LS258B
$\overline{E}_O$	S	I_0	I_1	Z	$\overline{Z}$
H	X	X	X	(Z)	(Z)
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (off)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage		2.4	3.1		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage			0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
				0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current — HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current — LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current Other Inputs S Inputs				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Other Inputs S Inputs				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current All Inputs				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH	LS257B LS258B			10 9.0	mA	V_{CC} = MAX	
	Total, Output LOW	LS257B LS258B			16 14	mA		
	Total, Output 3-State	LS257B LS258B			19 16	mA		

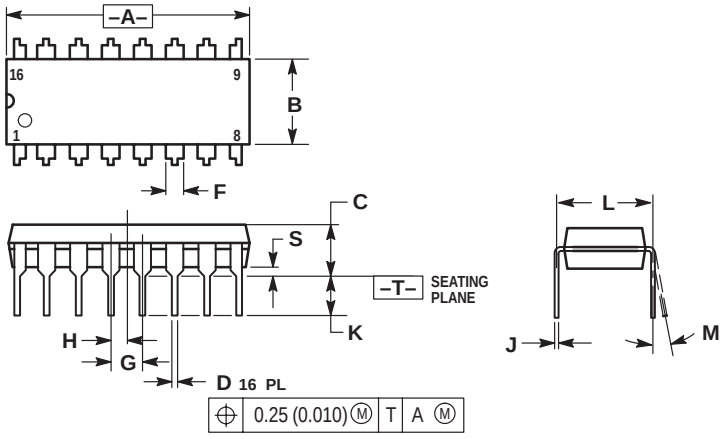
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V) See SN74LS251 for Waveforms

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 12	13 15	ns	Figures 1 & 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		14 14	21 21	ns	Figures 1 & 2	
t_{PZH}	Output Enable Time to HIGH Level		20	25	ns	Figures 4 & 5	C_L = 45 pF R_L = 667 Ω
t_{PZL}	Output Enable Time to LOW Level		20	25	ns	Figures 3 & 5	
t_{PLZ}	Output Disable Time to LOW Level		16	25	ns	Figures 3 & 5	C_L = 5.0 pF R_L = 667 Ω
t_{PHZ}	Output Disable Time from HIGH Level		18	25	ns	Figures 4 & 5	

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

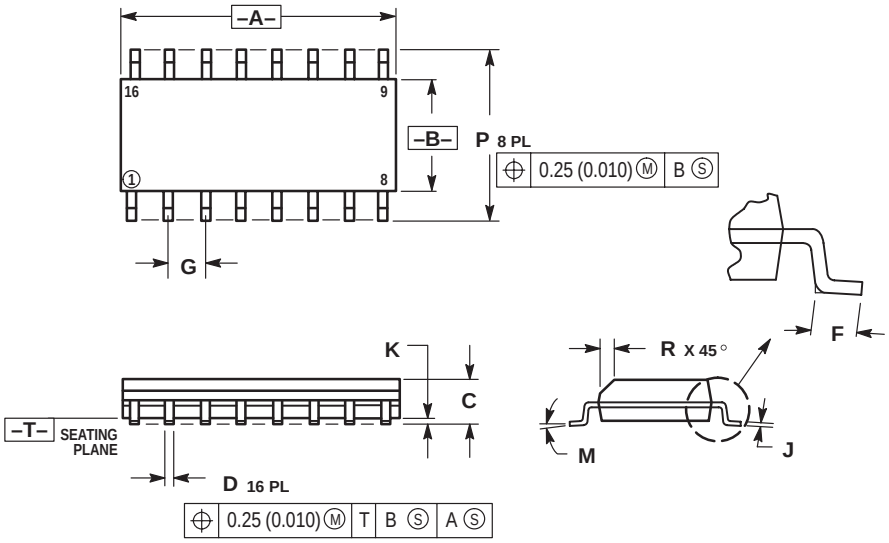


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

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