

## High Speed CMOS Logic Dual 4-Stage Static Shift Register

### Features

- **Maximum Frequency, Typically 60MHz**  
 $C_L = 15\text{pF}$ ,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$
- **Positive-Edge Clocking**
- **Overriding Reset**
- **Buffered Inputs and Outputs**
- **Fanout (Over Temperature Range)**
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- **Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$

### Description

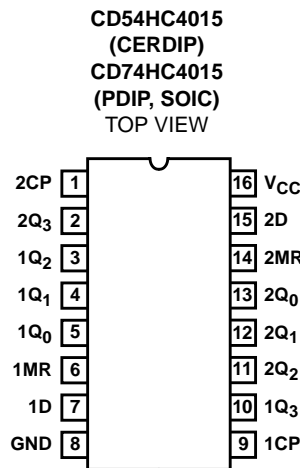
The 'HC4015 consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent Clock (CP) and Reset (MR) inputs as well as a single serial Data input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the Data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line.

The device can drive up to 10 low power Schottky equivalent loads. The 'HC4015 is an enhanced version of equivalent CMOS types.

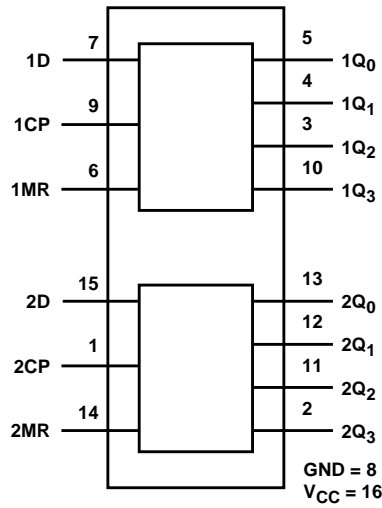
### Ordering Information

PART NUMBER	TEMP. RANGE ( $^\circ\text{C}$ )	PACKAGE
CD54HC4015F3A	-55 to 125	16 Ld CERDIP
CD74HC4015E	-55 to 125	16 Ld PDIP
CD74HC4015M	-55 to 125	16 Ld SOIC

### Pinout



**Functional Diagram**



**TRUTH TABLE**

INPUTS			OUTPUTS			
CP	D	R	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
↑	l	L	L	q' <sub>0</sub>	q' <sub>1</sub>	q' <sub>2</sub>
↑	h	L	H	q' <sub>0</sub>	q' <sub>1</sub>	q' <sub>2</sub>
↓	X	L	q' <sub>0</sub>	q' <sub>1</sub>	q' <sub>2</sub>	q' <sub>3</sub>
X	X	H	L	L	L	L

H = High Voltage Level

h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition

L = Low Voltage Level

l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition

X = Don't Care.

↑ = Low to High Clock Transition

↓ = High to Low Clock Transition

q'<sub>n</sub> = Lower case letters indicate the state of the referenced output one set-up time prior to the Low to High clock transition.

## CD54HC4015, CD74HC4015

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package .....	67
M (SOIC) Package .....	73
Maximum Junction Temperature .....	150 $^{\circ}C$
Maximum Storage Temperature Range .....	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	300 $^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range, $T_A$ .....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	100ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
			-4	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
			4	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$	
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$	

## CD54HC4015, CD74HC4015

### Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Maximum Clock Frequency	f <sub>MAX</sub>	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
Clock Pulse Width	t <sub>W</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
MR Pulse Width	t <sub>W</sub>	2	150	-	190	-	225	-	ns
		4.5	30	-	38	-	45	-	ns
		6	26	-	33	-	38	-	ns
MR Recovery Time	t <sub>REC</sub>	2	50	-	65	-	75	-	ns
		4.5	10	-	13	-	15	-	ns
		6	9	-	11	-	13	-	ns
Set-up Time, Data-In to CP	t <sub>SUL</sub> , t <sub>SUH</sub>	2	60	-	75	-	90	-	ns
		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns
Hold Time, Data-In to CP	t <sub>H</sub>	2	0	-	0	-	0	-	ns
		4.5	0	-	0	-	0	-	ns
		6	0	-	0	-	0	-	ns

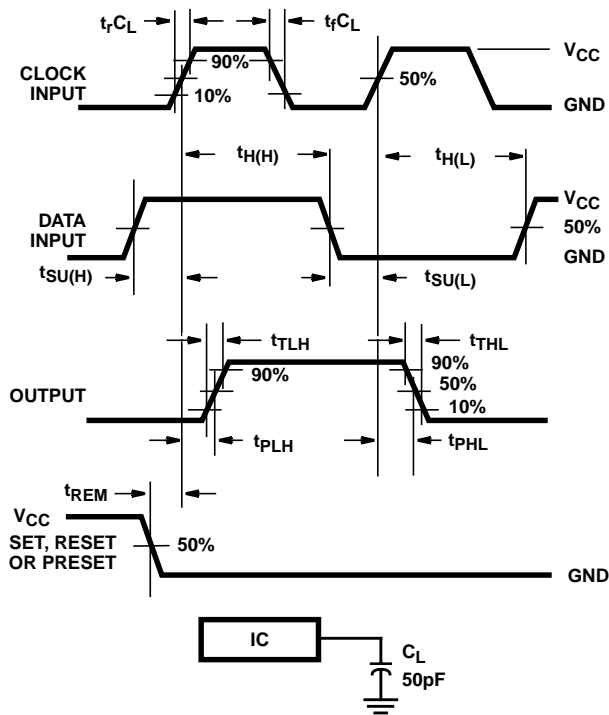
### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay (Figure 1) Clock to Q <sub>n</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	175	-	220	-	270	ns
			4.5	-	-	35	-	44	-	54	ns
		C <sub>L</sub> = 15pF	5	-	14	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	30	-	37	-	46	ns
MR to Q <sub>n</sub> , (Clock High)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	64	-	83	ns
		C <sub>L</sub> = 15pF	-	-	25	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	47	-	54	-	71	ns
MR to Q <sub>n</sub> , (Clock Low)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	325	-	400	-	490	ns
			4.5	-	-	65	-	81	-	98	ns
		C <sub>L</sub> = 15pF	-	-	25	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	55	-	69	-	83	ns
Output Transition Time (Figure 1)	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>IN</sub>	C <sub>L</sub> = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f <sub>MAX</sub>	C <sub>L</sub> = 15pF	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 2, 3)	C <sub>PD</sub>	C <sub>L</sub> = 15pF	5	-	43	-	-	-	-	-	pF

#### NOTES:

2. C<sub>PD</sub> is used to determine the dynamic power consumption, per shift register.
3. P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ C<sub>L</sub> V<sub>CC</sub><sup>2</sup> where f<sub>i</sub> = Input Frequency, C<sub>L</sub> = Output Load Capacitance, V<sub>CC</sub> = Supply Voltage.

**Test Circuit and Waveform**



**FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-8995301EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC4015F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC4015E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4015EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4015M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4015ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4015MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

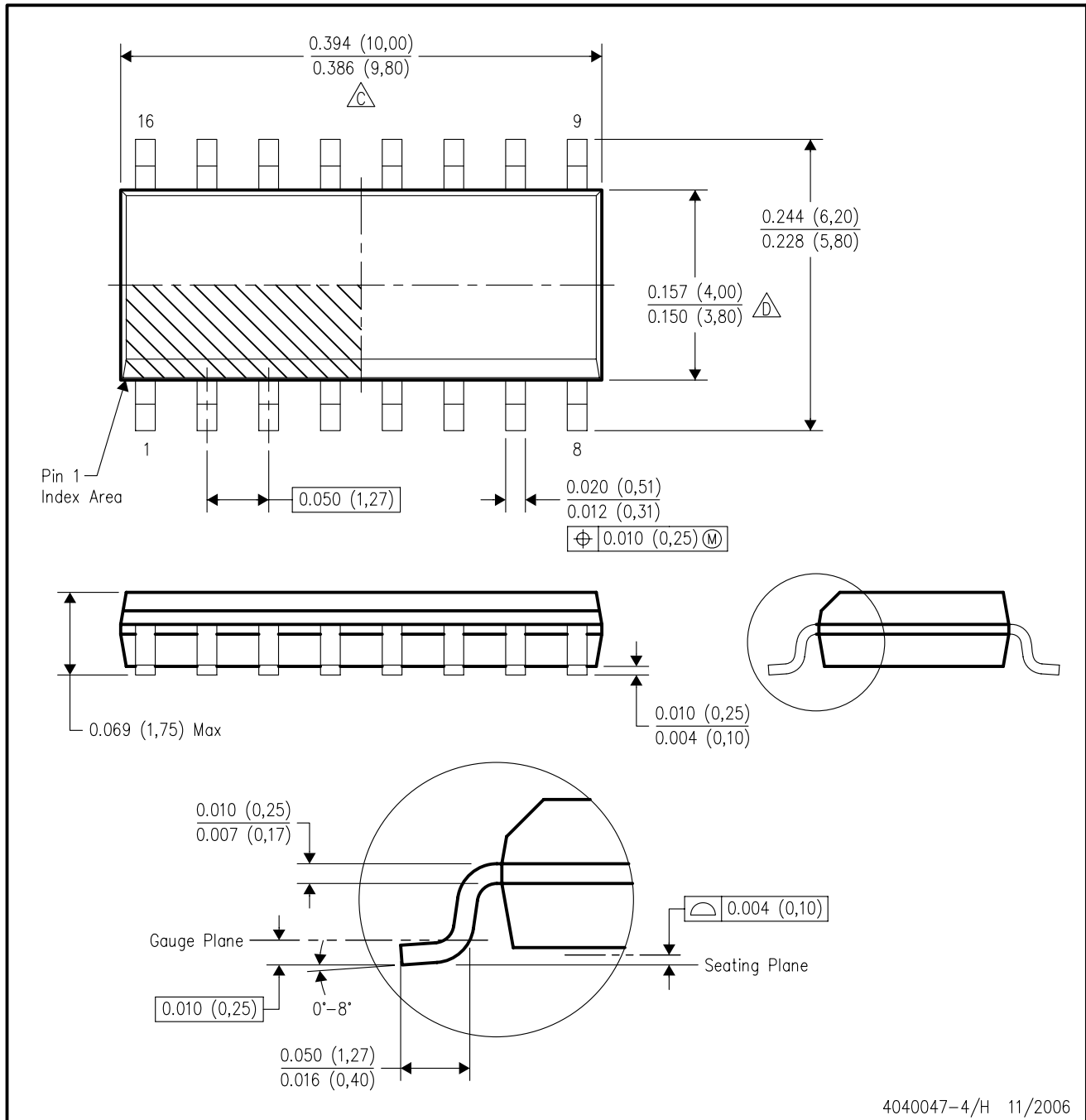


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

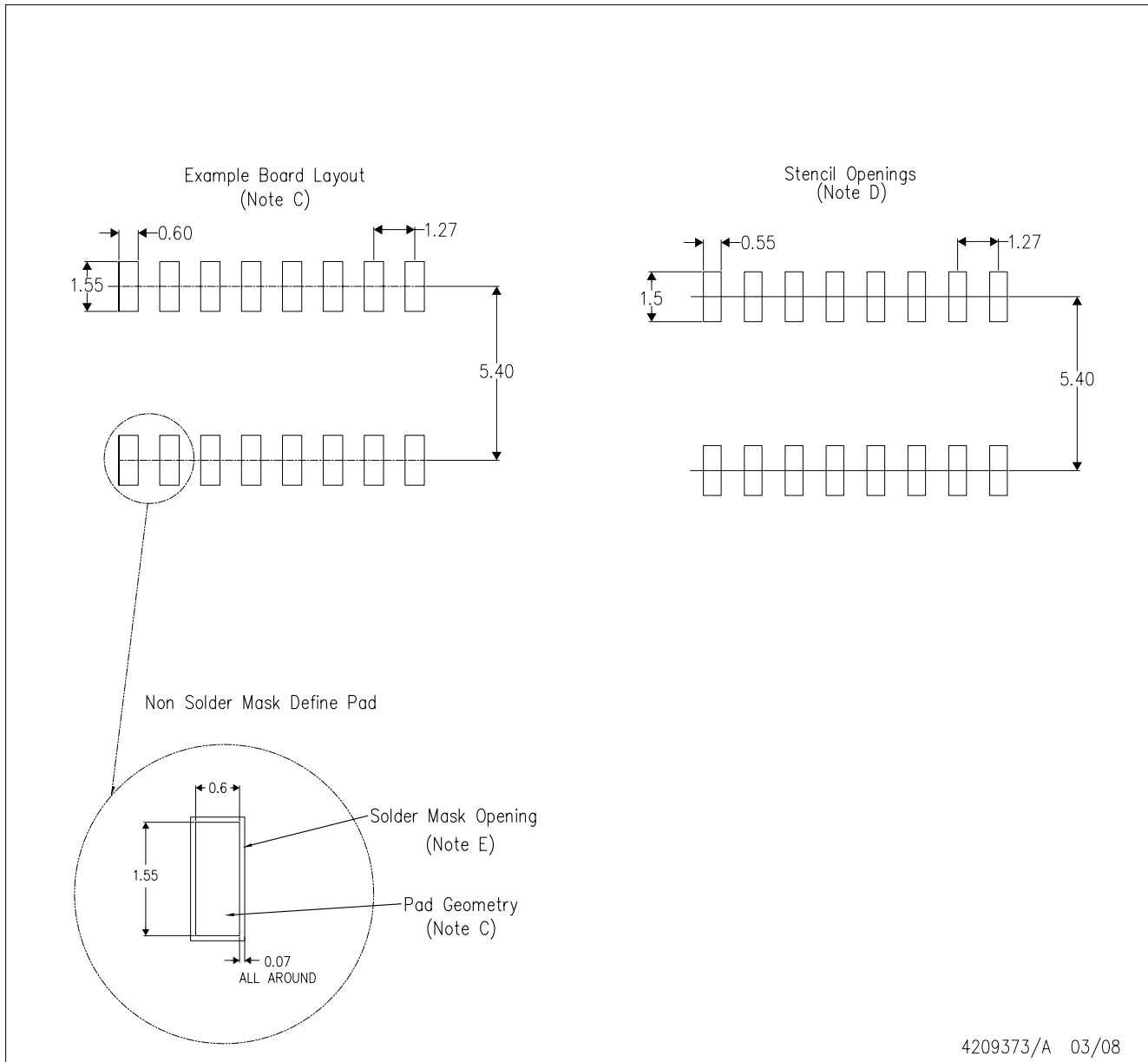


4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.



D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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